Embedded Parallel Computing

Lecture 3 - Multiprocessors Interconnection Networks

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Course webpage:: <http://www.hh.se/DO8003>
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- Static
  - 1D, 2D, Hypercube
- Dynamic
  - Bus-based
    - Single - Multiple buses
  - Switch-based
    - Single stage, Multi-stage, Crossbar

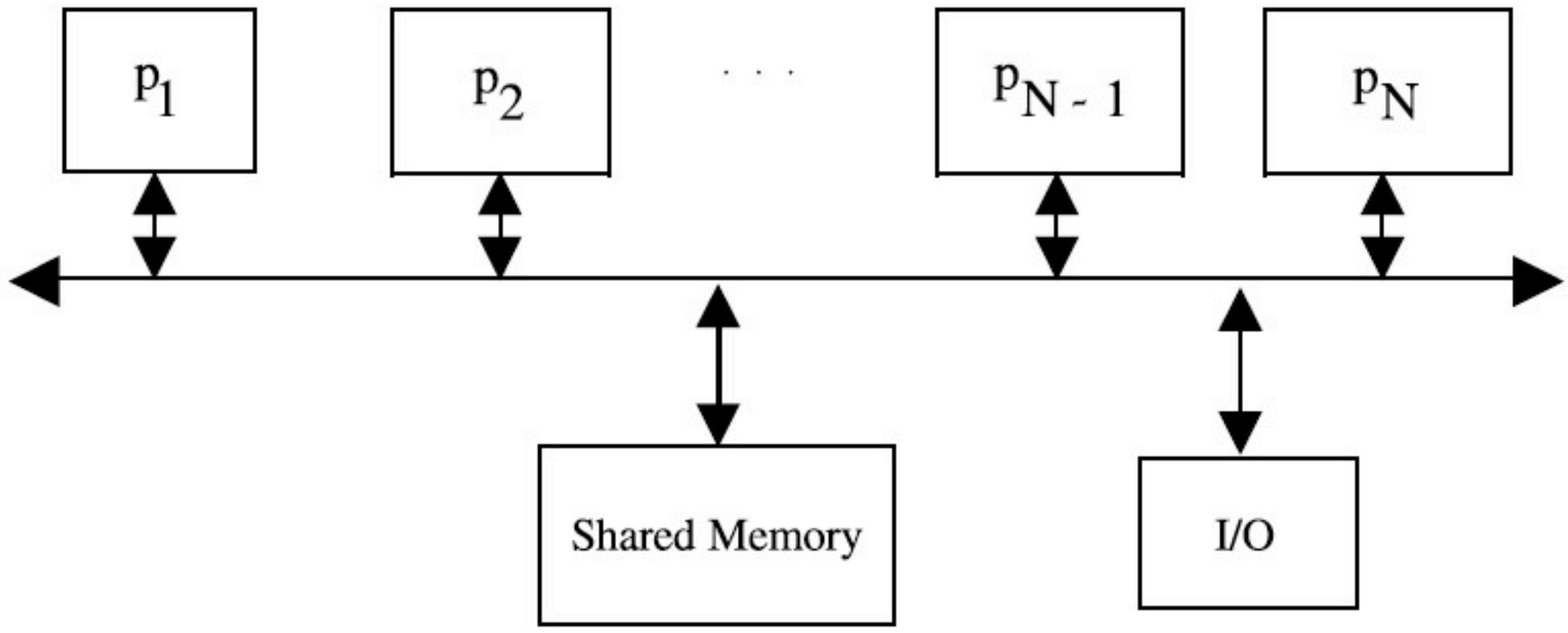
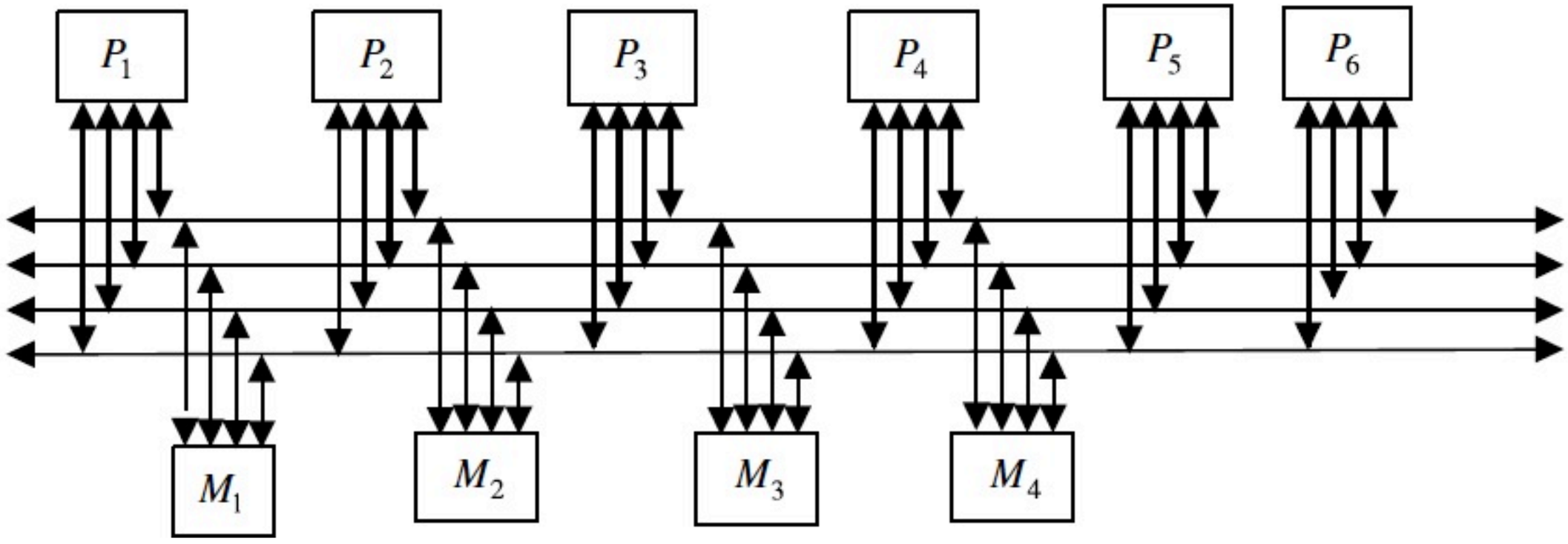


Figure 2.2 Example single bus system.


P_1
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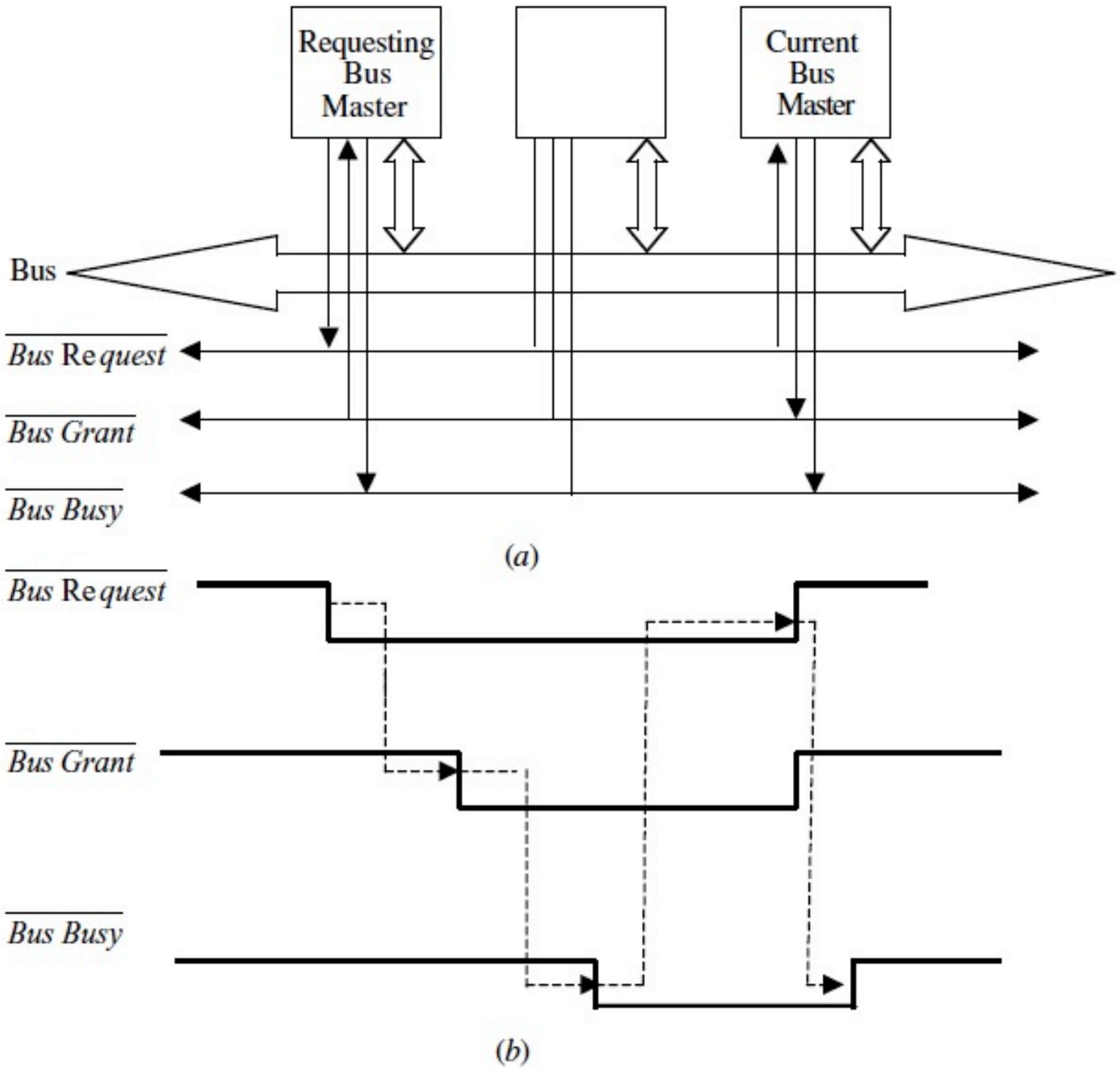
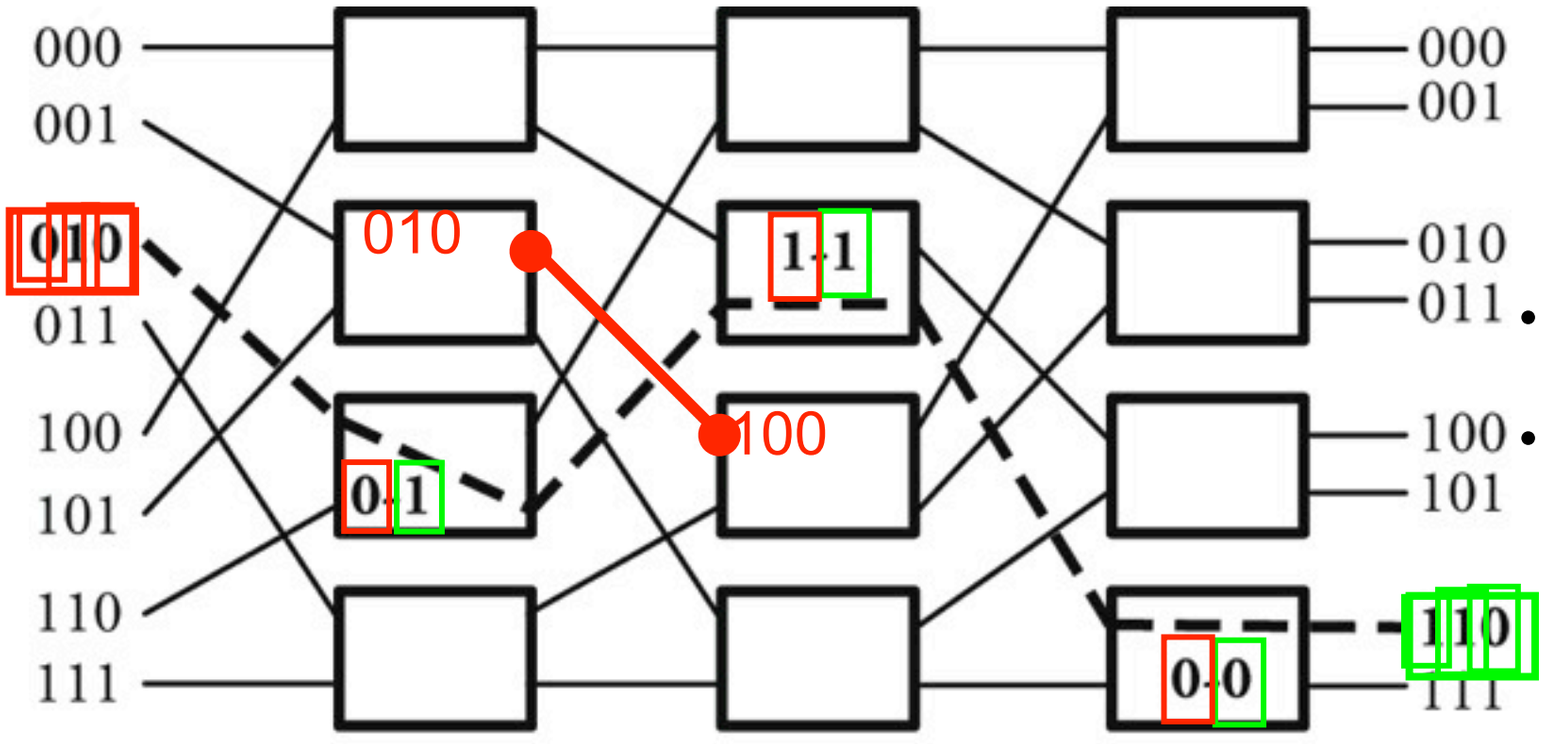


Figure 2.4 Bus handshaking mechanism (*a*) the scheme; and (*b*) the timing.

Characterization of Direct Networks

- Traditionally modeled by graphs: G(N,C)
  - G = graph
  - N = vertices of graph G represent set of processing nodes
  - C = edges of graph G represent set of communication channels
- Basic network properties
  - **Node degree** = nbr of channels connecting node to its neighbour
  - **Diameter** = maximum distance between 2 nodes in the network
  - **Regularity** = a network is regular when all nodes have the same degree
  - **Symmetry** = a network is symmetric when it looks alike from every node

Blocking Switch Fabrics: Omega network Ω



- One route between each input and output
- 2^k = N inputs and outputs
- $\log_2 N$ stages each having N/2 exchange elements
- Perfect shuffle connection system before each stage
  - Interconnection link starting at the output number of a given crossbar stage ends at the input of the next crossbar stage with the same number but one ”bit step” rotated left
- Direct connection from last stage o destination
- Selfrouting: comparing bit-by-bit between source and destination address
  - Same bit: message passed through
  - Different bit: message is crossed over

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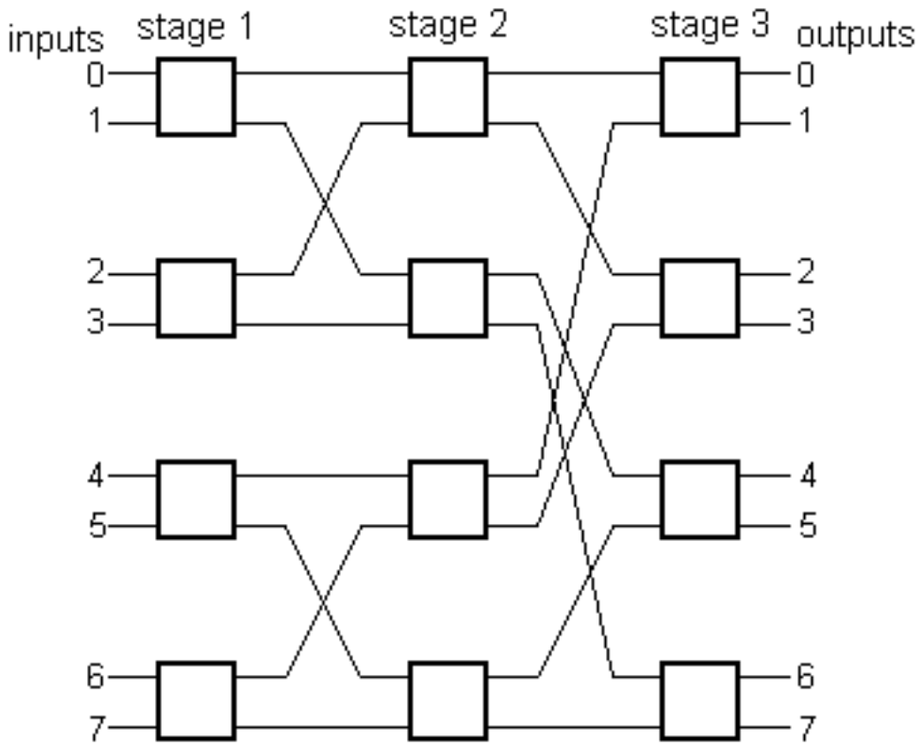
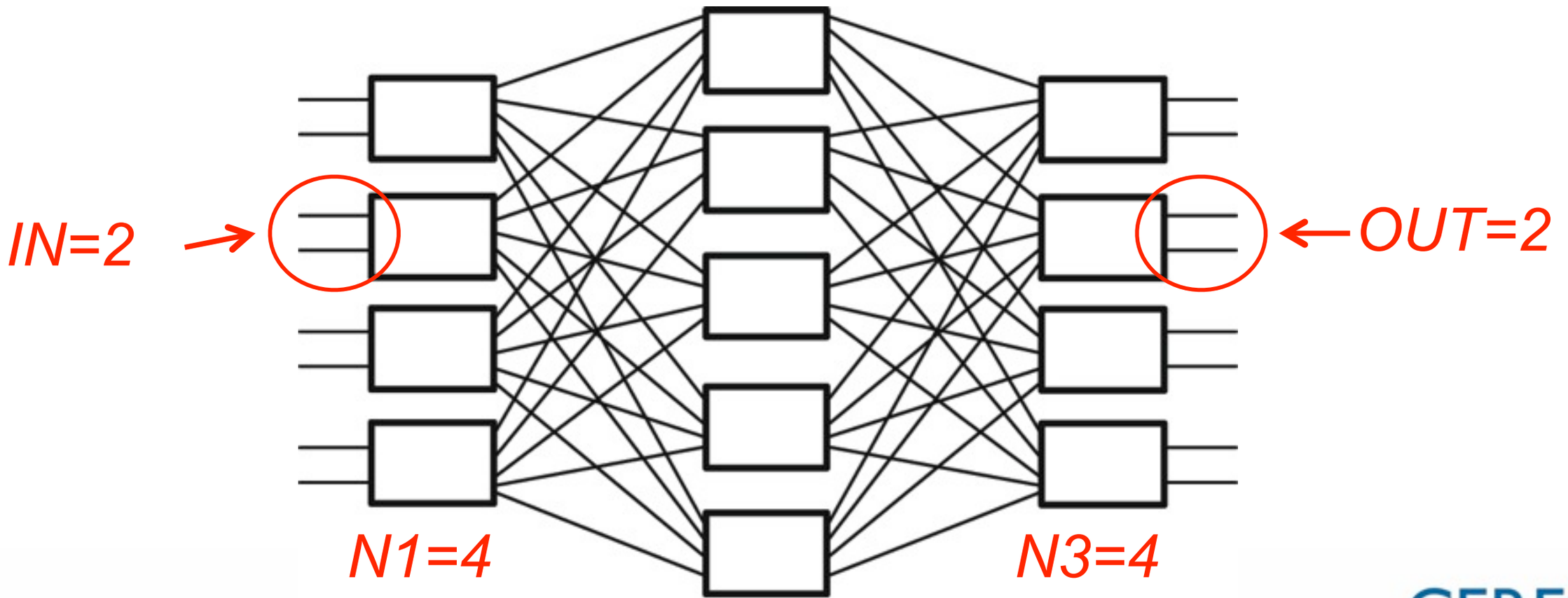


Nonblocking Switch Fabrics: Clos network

- 3 stages
  - fully connected between stage 1 and 2
  - fully connected between stage 2 and 3
- All switches in first (last) stage have same number of input (output) lines
- A clos network is fully specified by (*IN, N1, N2, N3, OUT*).



Nonblocking Switch Fabrics: Clos network

Theorems:

”A Clos network built from strictly nonblocking modules is itself strictly nonblocking if

$N2 \geq IN+OUT-1$

That condition is necessary if $N1 \geq OUT$ and $N3 \geq IN$.”

> ”A Clos network built from rearrangeably nonblocking modules is itself rearrangeably nonblocking if and only if
>
> $N2 \geq \max(IN,OUT)$.”

Interconnection Networks

Computer Architecture: A Quantitative Approach
4th Edition, Appendix E

Timothy Mark Pinkston

University of Southern California

http://ceng.usc.edu/smart/slides/appendixE.html

José Duato

Universidad Politécnica de Valencia

http://www.gap.upv.es/slides/appendixE.html

...with major presentation contribution from José Flich, UPV
(and Cell BE EIB slides by Tom Ainsworth, USC)

Questions

- Study-support questions

Links

Microprocessor Design <http://en.wikibooks.org/wiki/Microprocessor_Design>

Computer Network <http://en.wikipedia.org/wiki/Computer_network>
Network Topology <http://en.wikipedia.org/wiki/Network_topology>

Network-on-chip (NoC) <http://en.wikipedia.org/wiki/Network_On_Chip>

Interconnection networks
<http://en.wikipedia.org/wiki/Network_topology>
http://en.wikipedia.org/wiki/Multistage_interconnection_networks
http://en.wikipedia.org/wiki/Omega_network
http://en.wikipedia.org/wiki/Banyan_network
http://en.wikipedia.org/wiki/Nonblocking_minimal_spanning_switch
http://www.cs.cf.ac.uk/Parallel/Year2/section5.html
http://pnewman.com/papers/thesis/chapter4.pdf
http://www.cs.illinois.edu/class/sp11/cs533/notes/InterconnectionNet.pdf
http://www.ece.gatech.edu/academic/courses/fall2006/ece6100/Lectures/Module%2013%20-%20Networks/module.interconnection.networks.pdf

Pinkston & Duato, Interconnection Networks; Appendix E; Computer Architecture: A Quantitative Approach 4th Edition, <http://ceng.usc.edu/smart/slides/appendixE.html>