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3 pages

Written Exam
Embedded Parallel Computing (DO8003)

March 15, 2010

Closed book exam.

Aids allowed: A dictionary, translating between English and your native language, or an English Thesaurus. It must be in printed form, not electronic!

Welcome to the exam!

READ THIS FIRST:

In most of the assignments in this exam you are asked to "describe" or "explain". Please write short and concise. It is not necessary that you cover everything that can possibly be connected to the topic – it is more important that what you write is clear, coherent, correct and relevant.

The facts that you find in the course literature are not "the law". If you have different opinion, don't be afraid to mention it. Of course, you are also free to take up things that are not to be found in the course literature, as long as they are of importance to the topic.

Please, read the assignments carefully, so that you give answer to the correct questions – and to all questions!

Answer in English or Swedish – whichever you prefer!

Good luck!

-- *Bertil*

Number of assignments: 5
Maximum points: 46
Bonus points from the seminars (maximum 21) will be added to the points of this written exam.

Required points:	33	44	55
Grade:	3	4	5

Grades may be raised based on excellent seminar achievements.

Assignment 1: Combine Concepts (6 p)

Combine each of the concepts 1 - 6 with the correct description or property A - L
(Only one description/property per concept)

1. NUMA
2. Superscalar processor
3. Load delay cycle
4. Multicomputer
5. VLIW
6. Cube-connected cycles

A. Used to synchronise SIMD processing elements
B. Memory is not shared
C. A three-dimensional microarchitecture
D. More than one instruction can be started each clock cycle
E. High-speed memory needs to grow faster than the number of PEs
F. Packet switching technique where message pieces are pipelined through the net
G. The compiler detects the instruction level parallelism
H. Can hopefully be filled with an other instruction
I. Prerequisite for high performance in SIMD architectures
J. Causes the growing processor-memory gap
K. The advantage is that all nodes have exactly three neighbours
L. Distributed shared-memory architecture

Assignment 2: MIMD Architecture (8 p)

a) Why is latency an inherent problem in shared-memory computers? How can multithreading help to reduce the negative consequences?

b) Compare write-through and write-back caches in multiprocessors. What are the pros and cons of each?

Assignment 3: Static Interconnection Networks (12 p)

You are hardware designer in a multiprocessor company and are asked to recommend interconnection network for two future products, both with a private memory (message passing) architecture. One of the products will have at least 100 processors (you may choose a suitable number), the other one at least 500 processors (choose a suitable number). The topologies that you may choose among are: binary tree, 2-dimensional mesh, and *n*-dimensional hypercube.

a) For each of the two products, and for all topologies, calculate the network's diameter and degree

b) Reason about what would be the best choice(s) for each of the products. In your reasoning you may include other criteria in addition to diameter and degree.

Assignment 4: Speedup and Efficiency (6 p)

Amdahl's law states the maximum *speedup* that can be achieved with n processors when the fraction f of the entire sequential work cannot be parallelized, while the rest can. The *efficiency* measure relates the speedup achieved to the ideal speedup.
a) Give the formulas for speedup and efficiency
b) For the following four cases, determine the maximum speedup and efficiency that can be achieved:
(i) $f = 0.1$, $n = 10$
(ii) $f = 0.1$, $n = 100$
(iii) $f = 0.01$, $n = 50$
(iv) $f = 0.005$, $n = 1000$

Assignment 5: Short Paper (14 p)

Choose **<u>one</u>** of the topics below. Recommended length: **2 - 3 pages**, including figures.

(Since this is an opportunity for you to choose the topic you know best, I will have quite high demands on the quality of your short paper when I mark it. So, please pay attention to how you organize it! And remember that it is not the length of the paper that gives you the points, it is the content!)

A. Data-parallel instructions in SIMD computers
In SIMD computers, instructions typically operate on arrays of data. Show how this is done by describing the roles of the host computer, the control unit and the processor array including memory. Give examples of typical SIMD instructions. How can the SIMD computer handle situations where the degree of parallelism in the data is larger than the number of processing elements? How does a bit-serial processor array handle data elements of any word length?

or

B. Dynamic interconnection networks
Many switched interconnection networks use 2x2 switches as building blocks. In this assignment you shall describe useful regular, multilayer network structures built from such switches. You shall also describe the capabilities and limitations of these networks as well as how the switch settings in the network are found based on the destination address. Your description should be accompanied by proofs/arguments as well as by illustrative examples.

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