Efficient Parallel Architectures for Future Radar Signal Processing

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Abstract

The processing demands on future embedded radar signal processors may stretch to several trillions of floating-point operations per second (TFLOPS). This is an increase of two to three orders of magnitude relative to the requirements of today. Still, the tight size and power constraints are unchanged. To meet this, new, highly parallel computer systems are needed. The systems should efficiently deliver very high performance, as well as being general enough. Another challenge for future signal processors is the requirement for having huge working memories that are accessed in complicated patterns.

This thesis analyses the challenges of two classes of radar signal processing applications, namely Space-Time Adaptive Processing (STAP), which represents performance-intensive applications, and Synthetic Aperture Radar (SAR) processing, which represents memory-intensive applications. In addition to the actual performance and memory aspects of the applications, the desire for low-effort application development and maintenance is taken into consideration.

A multiple SIMD architecture is proposed for the STAP calculations. This architecture gives a combination of the high computational density in the SIMD processing modules with the overall flexibility provided on the system level. An embedded signal processing system based on the architecture is shown to be capable of TFLOPS class performance using standard CMOS VLSI technology available in the year 2001. The system is, for the given application domain, considered to have the same generality as commercial off-the-shelf (COTS) hardware, but has several years of time lead over COTS with regard to the computational performance.

The studied SAR processing is characterized by operating on huge data sets and having varying, non-linear data access paths. For this, algorithm solutions and execution schemes in interplay with a system parallelization approach are proposed. It is shown that it is possible to obtain efficient memory accesses, despite the complicated memory access patterns. It is also shown that the computational burden from complex interpolation kernels can be reduced through extensive calculation reuse.

Efficient engineering of complex applications in this context is discussed. The use of semi-transparent, platform-based development is demonstrated for STAP and SAR, and advocated for obtaining high engineering efficiency and long system sustainability, as well as high performance efficiency.

The overall conclusion drawn from this work is that a solid knowledge of the application domain and its future requirements, in combination with an understanding of its interaction with computational architectures, potentially enables several years of lead time in the realization of new, advanced signal processing products. The important requirements on programmability and sustainability must also be taken into account in order to achieve a viable signal processing solution.

Keywords: computer architecture, radar signal processing, space-time adaptive processing, synthetic aperture radar, parallel processing, engineering efficiency.