Courseinformation Hardware Design using VHDL, 7.5 credits Semester1 2010

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Homepage: https://www.hh.se/et6001

Course literature: Sjoholm and Lindh: VHDL for Designers
Labs

Examination: Written exam. Written and oral presentation of and active participation in the project assignment. Approved lab segment.

Planning w. 35-42:

Lectures	22h	w. 35-39
Labs:	10h	w. 36-38
Project work:	6h	w. 40-42

Preliminary:

W35	**6h**	
Ch 1	Introduction and overview	p 1-13
Ch 2	Introduction to VHDL	p 15-28
Ch 3	Concurrent VHDL	p 30-31, 33-53, 56-59, 64-67
Ch 4	Sequential VHDL	p 71-101, 106-110
Introducing Lab1		
W36	**4h**	**Lab1 2h**
Ch 9	State machines	p 193-232
Ch 15	Design examples and design tips	p 327-351
Introducing Lab2		
W37	**4h**	**Lab2 4h**
	FPGA, PLD	
Ch 6	Structural VHDL	p 138-146
Ch 5	Library, package and subprograms	p 115-131
Introducing Lab3		
W38	**4h**	**Lab3 4h**
Ch 14	Common design errors in VHDL and how to avoid them	p 318-326
Ch 8	Testbench	p 163-171, 178-179
W39h		
Ch 11	Design methodology	
Ch 7	RAM and ROM	p 158-162
Guestlecture		
Introducing project work		
W40-42	**Consulting 2h/week**	
Project work		