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3 pages

Written Exam
Parallel Computer Architecture (DO8001)

January 7, 2008, 09.00 - 13.00

Closed book exam.

Aids allowed: A dictionary, translating between English and your native language, or an English Thesaurus. It must be in printed form, not electronic!

Welcome to the exam!

READ THIS FIRST:

In most of the assignments in this exam you are asked to "describe" or "explain". Please write short and concise. It is not necessary that you cover everything that can possibly be connected to the topic – it is more important that what you write is clear, coherent, correct and relevant.

The facts that you find in the course literature are not "the law". If you have different opinion, don't be afraid to mention it. Of course, you are also free to take up things that are not to be found in the course literature, as long as they are of importance to the topic.

Please, read the assignments carefully, so that you give answer to the correct questions – and to all questions!

Good luck!

-- Bertil

Number of assignments: 5
Maximum points: 60
Bonus points from the seminars (maximum 32) will be added to the points of this written exam.

Required points:	40	60	75
Grade:	3	4	5

Grades may be raised based on excellent seminar achievements.

Assignment 1: Combine Concepts (7 p)

Combine each of the concepts 1 - 7 with the correct description or property A - M
(Only one description/property per concept)

1. Cube-connected cycles
2. Cut-through
3. Superscalar processor
4. Load delay cycle
5. Benes network
6. Binary tree network
7. VLIW

A. Used to synchronise SIMD processing elements
B. Non-blocking, multi-stage type
C. Diameter grows as 2-logarithm of number of nodes
D. An open-source microarchitecture
E. Benefits from out-of-order execution
F. Packet switching technique where message pieces are pipelined through the net
G. The compiler detects the instruction level parallelism
H. Can hopefully be filled with a piece of useful work
I. Technique for high performance in SIMD architectures
J. The latency in the interface between instruction cache and main memory
K. Causes the growing processor-memory gap
L. The advantage is that all nodes have exactly three neighbours
M. Distributed shared-memory architecture

Assignment 2: Contrast Concepts (9 p)

For each of the following concept-pairs, give a clear and concise explanation of **the significant difference**. (NOT a long description of each concept).
3 points per concept pair.

a) Instruction level parallelism vs. data parallelism
b) PRAM vs. MP-RAM
c) crossbar vs. multi-stage interconnection network

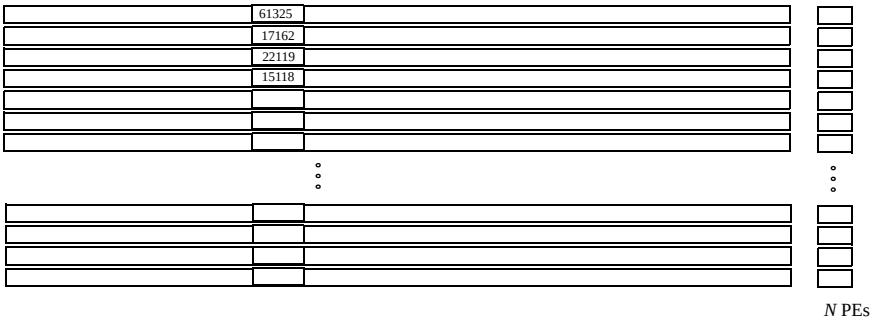
Assignment 3: SIMD Processing (12 p)

Assume that one field in the memory of a SIMD computer with *N* PEs stores integer values (as shown in the figure). The computer has *N* one-bit PEs, each with a one-bit wide interface to the memory.

Further, assume that we want to read out the numbers as a sorted list, starting with the largest number.

a. Describe (in words or in some kind of "pseudo-code") how this is done in the most efficient way.

b. Does the speed of the read-out (measured in numbers per second) depend on the value of *N*? Why?/Why not?



Assignment 4: VLIW Processors (12 p)

Assume that the intermediate-language code given below is to be executed on a VLIW processor.
(i) Draw the dataflow graph that shows the interdependencies between the instructions in the code.
(ii) Arrange the code – in the form of very long instruction words – for a processor with two adders, a multiplier, a load unit, and a store unit. The operation latencies are assumed to be one cycle, except for multiplication (two cycles) and load (two cycles). Do it in such a way that the execution time is minimized.
(Assume that bypassing is implemented both for arithmetic operations and for load/store instructions. If you make further assumptions, please clarify them).

```
I0   R3  <-- R1 * R2
I1   R6  <-- R4 + R5
I2   Load R7 <-- M[X]
I3   R8  <-- R7 + R6
I4   Store M[X]<--R8
I5   R9  <-- R2 + R3
I6   R10 <-- R2 + R8
I7   R11 <-- R7 * R9
I8   R12 <-- R8 * R10
I9   R13 <-- R4 + R8
```

Assignment 5: Cache Coherence (20 p)

First, motivate the use of caches in multiprocessors. Then describe the cache coherence problem and explain how the problem is solved using the “snooping on the bus” principle. Describe different variations of snooping protocols and discuss their pros and cons. Finally, describe how the cache coherence problem can be solved when other interconnection networks than a bus are used.

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