

SN54AHC541, SN74AHC541 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS261L – DECEMBER 1995 – REVISED FEBRUARY 2002

- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

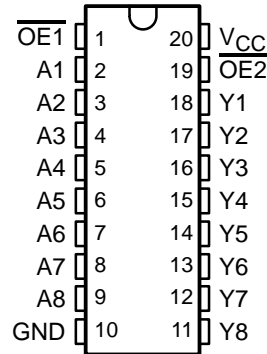
description

The 'AHC541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

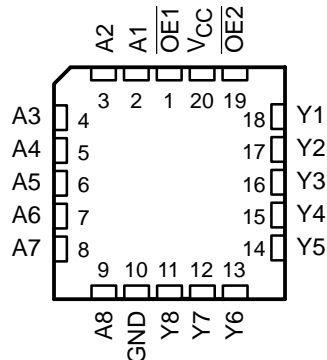
The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHC541 . . . J OR W PACKAGE
SN74AHC541 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC541 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AHC541N	SN74AHC541N
	SOIC – DW	Tube	SN74AHC541DW	AHC541
		Tape and reel	SN74AHC541DWR	
	SOP – NS	Tape and reel	SN74AHC541NSR	AHC541
	SSOP – DB	Tape and reel	SN74AHC541DBR	HA541
	TSSOP – PW	Tape and reel	SN74AHC541PWR	HA541
TVSOP – DGV	Tape and reel	SN74AHC541DGV	HA541	
-55°C to 125°C	CDIP – J	Tube	SNJ54AHC541J	SNJ54AHC541J
	CFP – W	Tube	SNJ54AHC541W	SNJ54AHC541W
	LCCC – FK	Tube	SNJ54AHC541FK	SNJ54AHC541FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

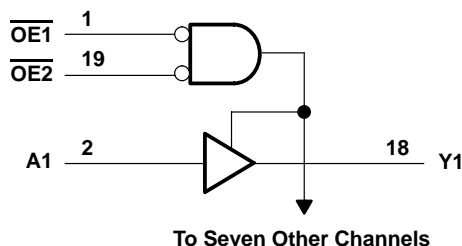
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FUNCTION TABLE
(each buffer/driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		SN54AHC541		SN74AHC541		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5		V
		V _{CC} = 3 V		2.1		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		V
		V _{CC} = 3 V		0.9		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50		μA
		V _{CC} = 3.3 V ± 0.3 V		-4		
		V _{CC} = 5 V ± 0.5 V		-8		
I _{OL}	Low-level output current	V _{CC} = 2 V		50		μA
		V _{CC} = 3.3 V ± 0.3 V		4		
		V _{CC} = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		ns/V
		V _{CC} = 5 V ± 0.5 V		20		
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC541		SN74AHC541		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
	I _{OL} = 8 mA	4.5 V			0.36		0.5	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{OZ} †	V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH}	5.5 V			±0.25		±2.5	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	40	μA	
C _i	V _I = V _{CC} or GND	5 V		2	10			10	pF	
C _o	V _O = V _{CC} or GND	5 V		4					pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† For input and output, I_{OZ} includes the input leakage current.



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC541		SN74AHC541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	5*	7*	1*	8.5*	1	8.5	ns	
t_{PHL}				5*	7*	1*	8.5*	1	8.5		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	6*	10.5*	1*	11*	1	11	ns	
t_{PZL}				6*	10.5*	1*	11*	1	11		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	7*	11*	1*	12*	1	12	ns	
t_{PLZ}				7*	11*	1*	12*	1	12		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	7.5	10.5	1	12	1	12	ns	
t_{PHL}				7.5	10.5	1	12	1	12		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	8	14	1	16	1	16	ns	
t_{PZL}				8	14	1	16	1	16		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	9	15.4	1	17.5	1	17.5	ns	
t_{PLZ}				9	15.4	1	17.5	1	17.5		
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1.5**				1.5	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC541		SN74AHC541		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.5*	5*	1*	6*	1	6	ns	
t_{PHL}				3.5*	5*	1*	6*	1	6		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.7*	7.2*	1*	8.5*	1	8.5	ns	
t_{PZL}				4.7*	7.2*	1*	8.5*	1	8.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	5*	7.5*	1*	8*	1	8	ns	
t_{PLZ}				5*	7.5*	1*	8*	1	8		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5	7	1	8	1	8	ns	
t_{PHL}				5	7	1	8	1	8		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.2	9.2	1	10.5	1	10.5	ns	
t_{PZL}				6.2	9.2	1	10.5	1	10.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6	8.8	1	10	1	10	ns	
t_{PLZ}				6	8.8	1	10	1	10		
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1**				1	ns	

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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC541		UNIT
	MIN	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}	0.8		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}	-0.8		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	4.7		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5		V
$V_{IL(D)}$ Low-level dynamic input voltage	1.5		V

NOTE 4: Characteristics are for surface-mount packages only.

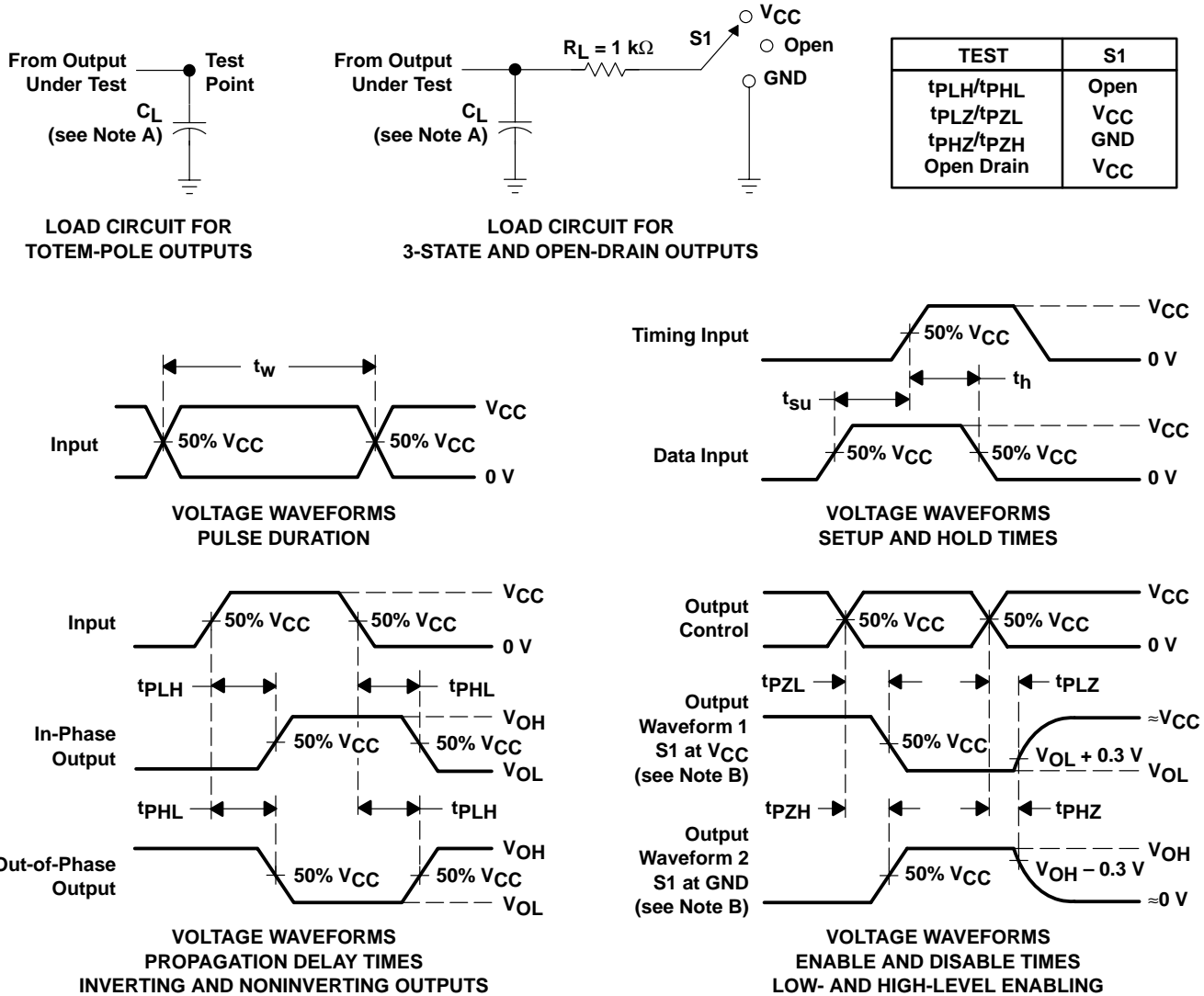
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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