ABSTRACT IDE0634

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Efficient Implementation of Stream Applications on Processor Arrays

Thesis for the degree of Licentiate of Engineering

This thesis concludes work conducted on exploring the usage of parallel and reconfigurable processor architectures in industrial high-performance embedded systems. This kind of systems has by tradition been built using a mix of digital signal processors and custom made hardware. Digital signal processors provide full functional flexibility, but at the cost of lower performance. Custom made hardware can be optimized for specific functions for high performance, but at the cost of inflexibility and high development costs. A desire is to combine flexibility and performance using commercial hardware, without trading too much of performance for flexibility.

Parallel and reconfigurable architectures provide a flexible computing space constituting processing elements that are coupled through configurable communication structures. Architectures designed with less complex processing elements render a high degree of utilizable parallelism at the cost of having to use a portion of the processing elements for control functions. In the thesis it is shown that it is possible to utilize this kind of architecture to achieve high performance efficiency, despite the fact that a large fraction of PEs are required to implement control-oriented portions in a fairly complex algorithm.

A major problem is that architectures of this kind expose a very complex programming abstraction for compilers and programmers. The approach taken in this work is a domain-specific stream processing model which provides means to express application-specific dataflows and computations in terms of streams. An extensive application study comprising the baseband processing in radio base stations has been used to define sufficient data types, operators and language constructs. Furthermore, to support industrial requirements on portability to different architectures, it must be possible to express parallelism and characteristic computations without exposing of hardware details in the source code.

To be able to prototype and set up experiments with stream processing languages an experimental programming framework has been developed. A first prototype language with specific primitive types, operators and stream constructs has been implemented in order to elaborate with baseband programing. It is demonstrated how these types and operators can be used to express machine-independent bit field and other fine-grained data parallel computations. Furthermore, the language has been designed with constructs for efficient and flexible programming of reconfiguration of distributed function parameters.

Keywords Parallel processing, reconfigurable architectures, stream processing, baseband.

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