

54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

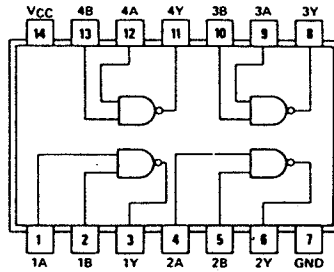
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

00

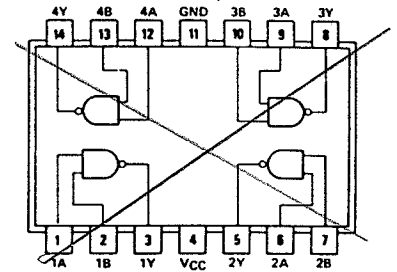
positive logic:

$$Y = \overline{AB}$$

See page 6-2



- | | |
|-----------------|-----------------|
| SN5400 (J) | SN7400 (J, N) |
| SN54ALS00A (J) | SN74ALS00A (N) |
| SN54AS00 (J) | SN74AS00 (N) |
| SN54HC00 (J) | SN74HC00 (N) |
| SN54LS00 (J, W) | SN74LS00 (J, N) |
| SN54S00 (J, W) | SN74S00 (J, N) |



SN5400 (W)

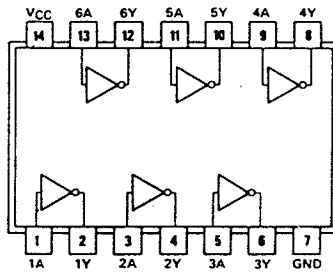
HEX INVERTERS

04

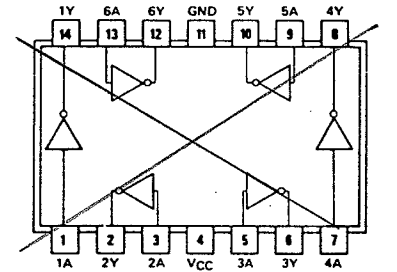
positive logic:

$$Y = \overline{A}$$

See page 6-2



- | | |
|-----------------|-----------------|
| SN5404 (J) | SN7404 (J, N) |
| SN54ALS04 (J) | SN74ALS04 (N) |
| SN54AS04 (J) | SN74AS04 (N) |
| SN54HC04 (J) | SN74HC04 (N) |
| SN54LS04 (J, W) | SN74LS04 (J, N) |
| SN54S04 (J, W) | SN74S04 (J, N) |



SN5404 (W)

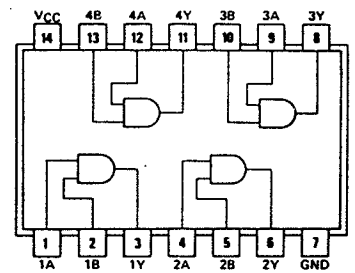
QUADRUPLE 2-INPUT POSITIVE-AND GATES

08

positive logic:

$$Y = AB$$

See page 6-10



- | | |
|-----------------|-----------------|
| SN5408 (J, W) | SN7408 (J, N) |
| SN54ALS08 (J) | SN74ALS08 (N) |
| SN54AS08 (J) | SN74AS08 (N) |
| SN54HC08 (J) | SN74HC08 (N) |
| SN54LS08 (J, W) | SN74LS08 (J, N) |
| SN54S08 (J, W) | SN74S08 (J, N) |

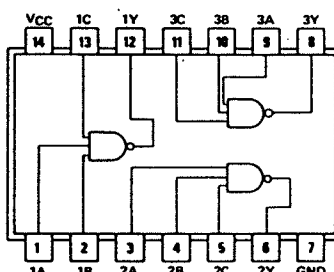
TRIPLE 3-INPUT POSITIVE-NAND GATES

10

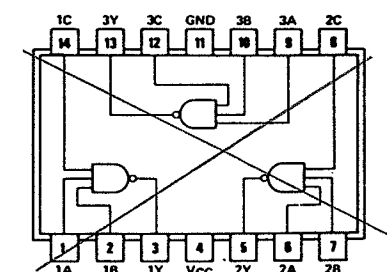
positive logic:

$$Y = \overline{ABC}$$

See page 6-2



- | | |
|-----------------|-----------------|
| SN5410 (J) | SN7410 (J, N) |
| SN54ALS10 (J) | SN74ALS10 (N) |
| SN54AS10 (J) | SN74AS10 (N) |
| SN54HC10 (J) | SN74HC10 (N) |
| SN54LS10 (J, W) | SN74LS10 (J, N) |
| SN54S10 (J, W) | SN74S10 (J, N) |



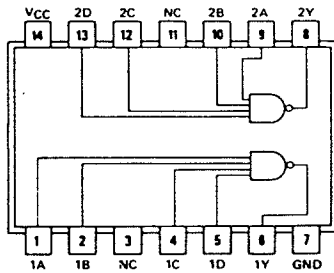
SN5410 (W)

DUAL 4-INPUT
POSITIVE-NAND GATES

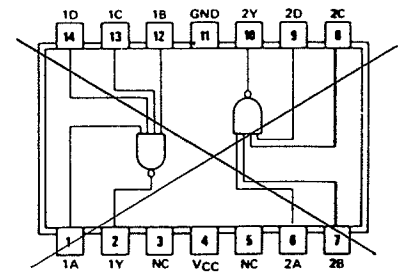
20

positive logic:
 $Y = \overline{ABCD}$

See page 6-2



- | | |
|-----------------|-----------------|
| SN5420 (J) | SN7420 (J, N) |
| SN54ALS20A (J) | SN74ALS20A (N) |
| SN54AS20 (J) | SN74AS20 (N) |
| SN54HC20 (J) | SN74HC20 (N) |
| SN54LS20 (J, W) | SN74LS20 (J, N) |
| SN54S20 (J, W) | SN74S20 (J, N) |



SN5420 (W)

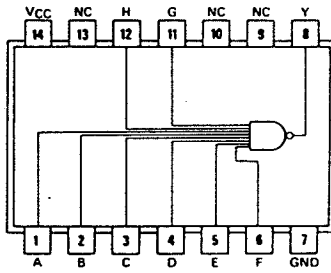
NC—No internal connection

8-INPUT
POSITIVE-NAND GATES

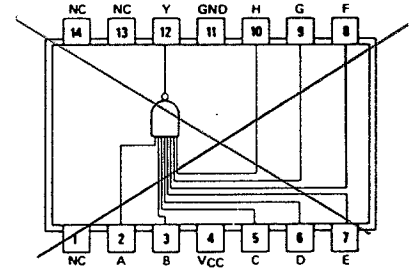
30

positive logic:
 $Y = \overline{ABCDEFGH}$

See page 6-2



- | | |
|-----------------|-----------------|
| SN5430 (J) | SN7430 (J, N) |
| SN54ALS30 (J) | SN74ALS30 (N) |
| SN54AS30 (J) | SN74AS30 (N) |
| SN54HC30 (J) | SN74HC30 (N) |
| SN54LS30 (J, W) | SN74LS30 (J, N) |
| SN54S30 (J, W) | SN74S30 (J, N) |



SN5430 (W)

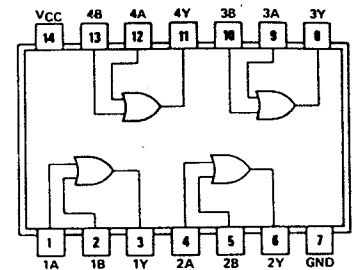
NC—No internal connection

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

32

positive logic:
 $Y = A+B$

See page 6-28



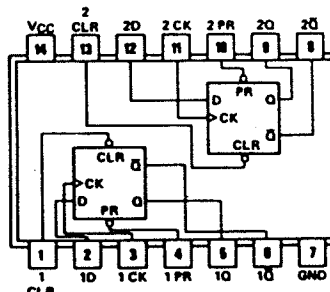
- | | |
|-----------------|-----------------|
| SN5432 (J, W) | SN7432 (J, N) |
| SN54ALS32 (J) | SN74ALS32 (N) |
| SN54AS32 (J) | SN74AS32 (N) |
| SN54HC32 (J) | SN74HC32 (N) |
| SN54LS32 (J, W) | SN74LS32 (J, N) |
| SN54S32 (J, W) | SN74S32 (J, N) |

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

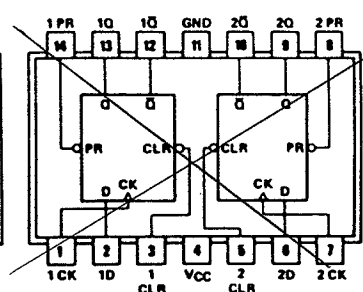
74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0



- | | |
|------------------|------------------|
| SN5474 (J) | SN7474 (J, N) |
| SN54ALS74 (J) | SN74ALS74 (N) |
| SN54AS74 (J) | SN74AS74 (N) |
| SN54HC74 (J) | SN74HC74 (N) |
| SN54LS74A (J, W) | SN74LS74A (J, N) |
| SN54S74 (J, W) | SN74S74 (J, N) |

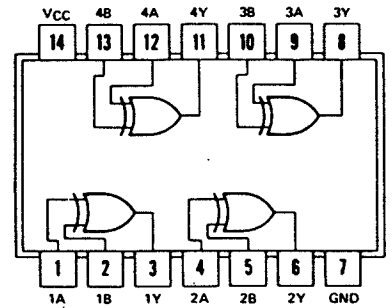


SN5474 (W)

See pages 6-46, 6-50, 6-54
and 6-56

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

86 $Y = A \oplus B = \bar{A}B + A\bar{B}$



- SN5486 (J, W) SN7486 (J, N)
- SN54ALS86 (J) SN74ALS86 (N)
- SN54HC86 (J) SN74HC86 (N)
- SN54LS86A (J, W) SN74LS86A (J, N)
- SN54S86 (J, W) SN74S86 (J, N)

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

See page 7-57

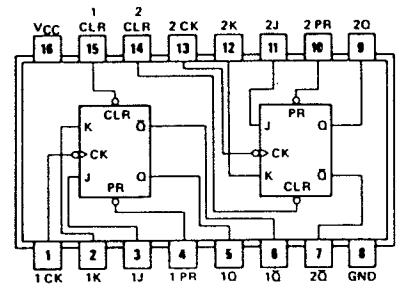
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

112

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q_0	\bar{Q}_0

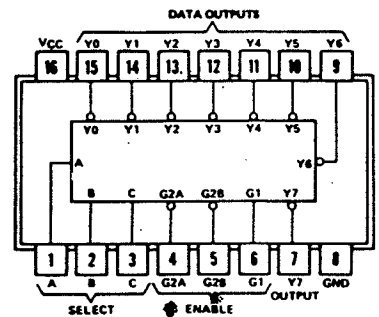
See pages 6-54 and 6-56



- SN54ALS112 (J) SN74ALS112 (N)
- SN54AS112 (J) SN74AS112 (N)
- SN54HC112 (J) SN74HC112 (N)
- SN54LS112A (J, W) SN74LS112A (J, N)
- SN54S112 (J, W) SN74S112 (J, N)

3-TO-8 LINE DECODERS/MULTIPLEXERS

138



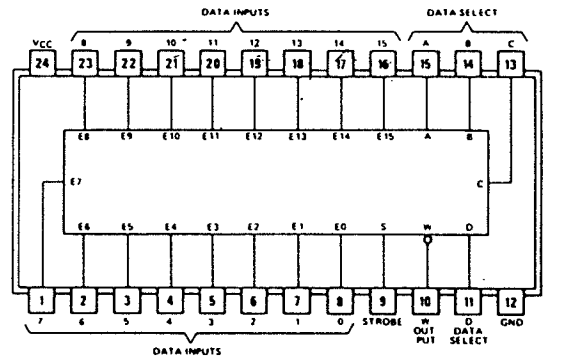
- SN54ALS138 (J, W) SN74ALS138 (N)
- SN54HC138 (J) SN74HC138 (N)
- SN54LS138 (J, W) SN74LS138 (J, N)
- SN54S138 (J, W) SN74S138 (J, N)

See page 7-124

1-OF-16 DATA SELECTORS/MULTIPLEXERS

150

See page 7-147

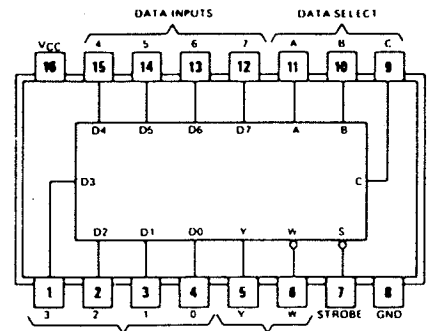


SN54150 (J, W)	SN74150 (J, N, NT)
SN54AS150 (J, JT)	SN74AS150 (N, NT)

1-OF-8 DATA SELECTORS/MULTIPLEXERS

151

See page 7-147



SN54151A (J, W)	SN74151A (J, N)
SN54ALS151 (J)	SN74ALS151 (N)
SN54AS151 (J)	SN74AS151 (N)
SN54HC151 (J)	SN74HC151 (N)
SN54LS151 (J, W)	SN74LS151 (J, N)
SN54S151 (J, W)	SN74S151 (J, N)

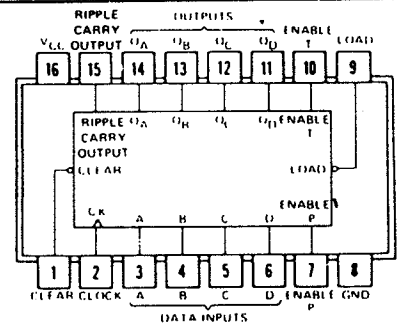
SYNCHRONOUS 4-BIT COUNTERS

160 DECADE, DIRECT CLEAR

161 BINARY, DIRECT CLEAR

162 DECADE, SYNCHRONOUS CLEAR

163 BINARY, SYNCHRONOUS CLEAR



SN54160 (J, W)	SN74160 (J, N)	SN54ALS162B (J)	SN74ALS162B (N)
SN54ALS160B (J)	SN74ALS160B (N)	SN54AS162 (J)	SN74AS162 (N)
SN54AS160 (J)	SN74AS160 (N)	SN54HC162 (J)	SN74HC162 (N)
SN54HC160 (J)	SN74HC160 (N)	SN54LS162A (J, W)	SN74LS162A (J, N)
SN54LS160A (J, W)	SN74LS160A (J, N)	SN54S162 (J, W)	SN74S162 (J, N)
SN54161 (J, W)	SN74161 (J, N)	SN54163 (J, W)	SN74163 (J, N)
SN54ALS161B (J)	SN74ALS161B (N)	SN54ALS163B (J)	SN74ALS163B (N)
SN54AS161 (J)	SN74AS161 (N)	SN54AS163 (J)	SN74AS163 (N)
SN54HC161 (J)	SN74HC161 (N)	SN54HC163 (J)	SN74HC163 (N)
SN54LS161A (J, W)	SN74LS161A (J, N)	SN54LS163A (J, W)	SN74LS163A (J, N)
SN54162 (J, W)	SN74162 (J, N)	SN54S163 (J, W)	SN74S163 (J, N)

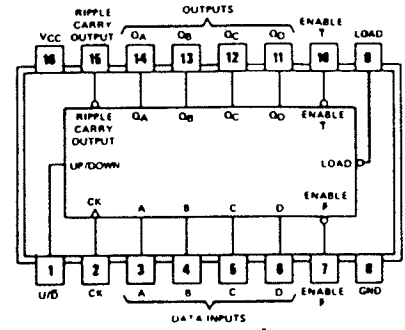
See page 7-177

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

168 DECADE

169 BINARY

See page 7-212

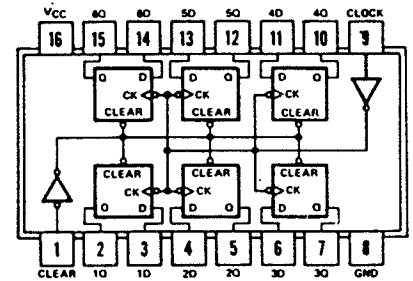


- | | |
|-------------------|-------------------|
| SN54S168 (J, W) | SN74S168 (J, N) |
| SN54LS169B (J, W) | SN74LS169B (J, N) |
| SN54S169 (J, W) | SN74S169 (J, N) |
| SN54ALS168A (J) | SN74ALS168A (N) |
| SN54ALS169A (J) | SN74ALS169A (N) |
| SN54AS168 (J) | SN74AS168 (N) |
| SN54AS169 (J) | SN74AS169 (N) |

HEX D-TYPE FLIP-FLOPS

174 SINGLE RAIL OUTPUTS
COMMON DIRECT CLEAR

See page 7-242

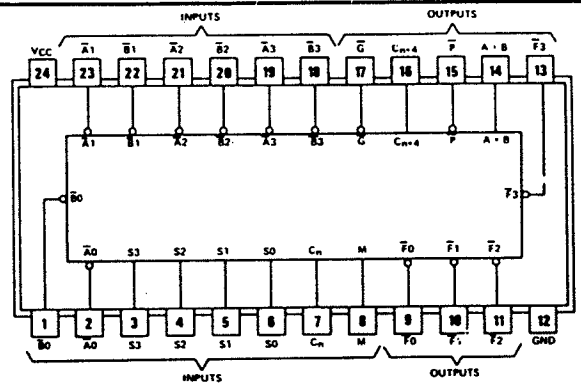


- | | |
|-------------------|------------------|
| SN54174 (J, W) | SN74174 (J, N) |
| SN54ALS174 (J, W) | SN74ALS174 (N) |
| SN54AS174 (J) | SN74AS174 (N) |
| SN54HC174 (J) | SN74HC174 (N) |
| SN54LS174 (J, W) | SN74LS174 (J, N) |
| SN54S174 (J, W) | SN74174 (J, N) |

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

181 16 ARITHMETIC OPERATIONS
16 LOGIC FUNCTIONS

See page 7-260



- | | |
|------------------|----------------------|
| SN54181 (J, W) | SN74181 (J, N, NT) |
| SN54LS181 (J, W) | SN74LS181 (J, N, NT) |
| SN54S181 (J, W) | SN74S181 (J, N, NT) |
| SN54AS181 (J) | SN74AS181 (N, NT) |

TYPES SN54LS138, SN54LS139A, SN54S138, SN54S139,
SN74LS138, SN74LS139A, SN74S138, SN74S139
DECODERS /MULTIPLEXERS

- Designed Specifically for High-Speed: Memory Decoders Data Transmission Systems
- 'S138 and 'LS138 3-to-8-Line Decoders Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
- 'S139 and 'LS139A Contain Two Fully Independent 2-to-4-Line Decoders/ Demultiplexers
- Schottky Clamped for High Performance

TYPE	TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC)	TYPICAL POWER DISSIPATION
'LS138	22 ns	32 mW
'S138	8 ns	245 mW
'LS139A	22 ns	34 mW
'S139	7.5 ns	300 mW

description

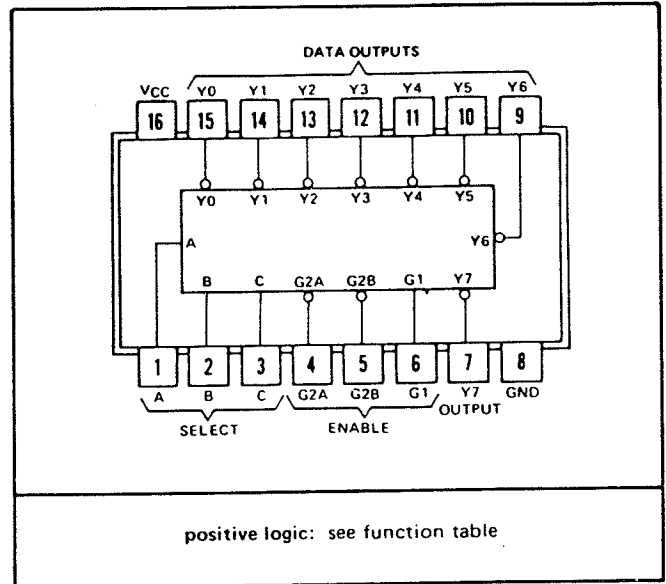
These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

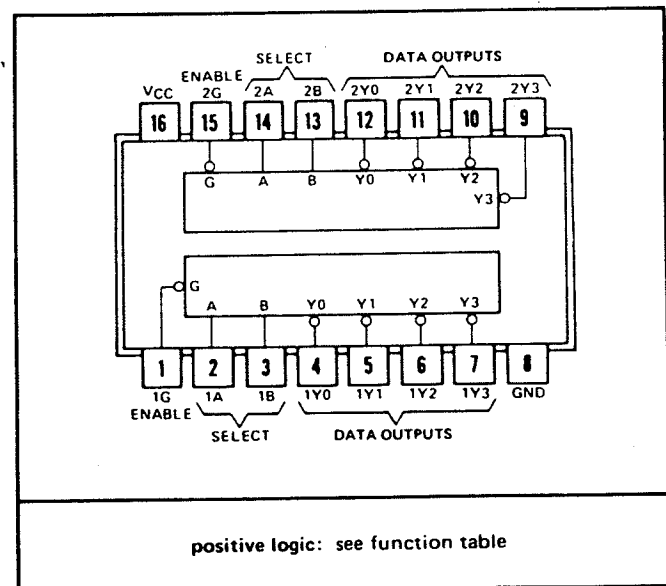
The 'LS139A and 'S139A comprise two individual two-line-to-four-line-decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74SL load ('LS138, 'LS139A) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design. Series 54LS and 54S devices are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74LS and 74S devices are characterized for 0°C to 70°C industrial systems.

SN54LS138, SN54S138 ... J OR W PACKAGE
SN74LS138, SN74S138 ... J OR N PACKAGE
(TOP VIEW)



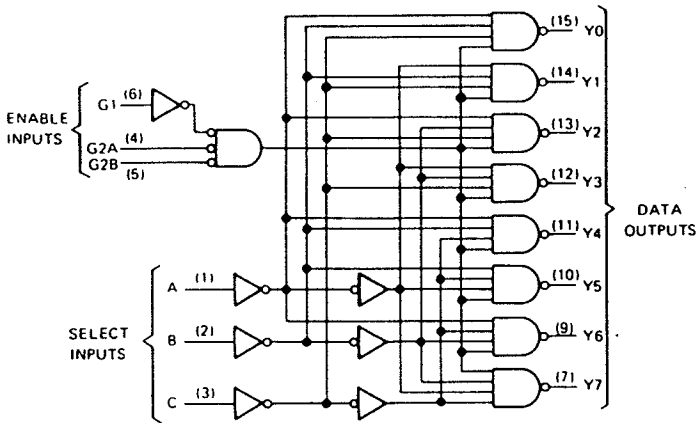
SN54LS139A, SN54S139 ... J OR W PACKAGE
SN74LS139A, SN74S139 ... J OR N PACKAGE
(TOP VIEW)



TYPES SN54LS138, SN54S138, SN54LS139A, SN54S139 SN74LS138, SN74S138, SN74LS139A, SN74S139 DECODERS/DEMULTIPLEXERS

functional block diagrams and logic

'LS138, 'S138



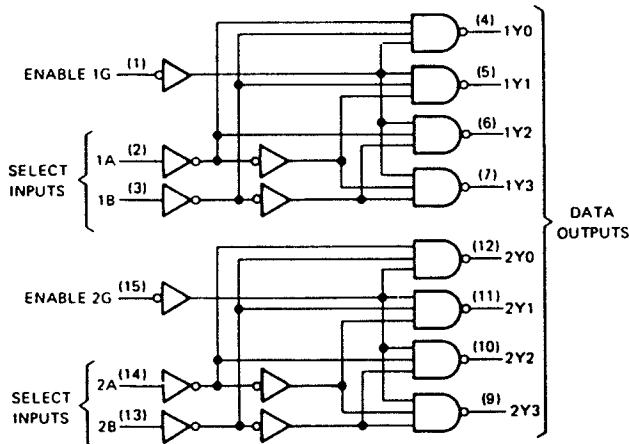
'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	L	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	H	L	H	H	L	H
H	L	H	H	L	H	H	H	H	L	H	L	H
H	L	H	H	H	H	H	H	H	H	L	L	H

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

'LS139A, 'S139

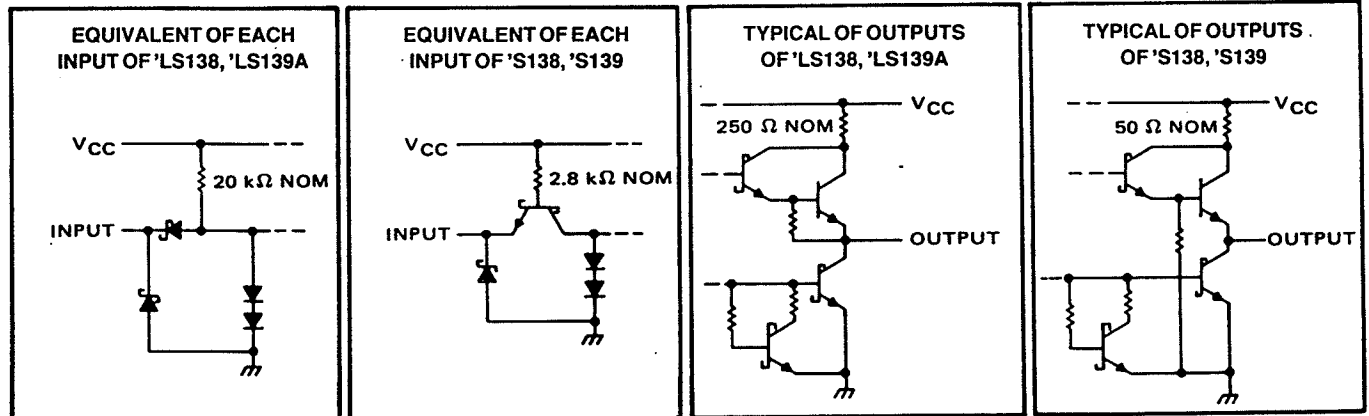


'LS139A, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

schematics of inputs and outputs



TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151 DATA SELECTORS/MULTIPLEXERS

DECEMBER 1972 - REVISED DECEMBER 1983

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	13 ns	200 mW
'151A	8 ns	145 mW
'152A	8 ns	130 mW
'LS151	13 ns	30 mW
'LS152	13 ns	28 mW
'S151	4.5 ns	225 mW

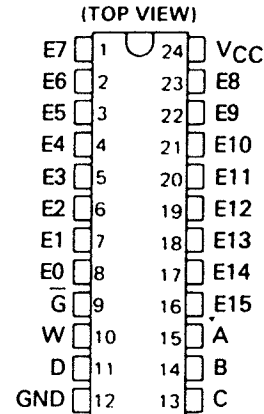
description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

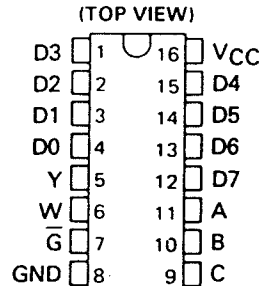
The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

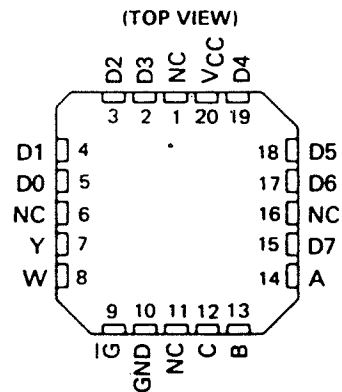
SN54150 ... J OR W PACKAGE
SN74150 ... J OR N PACKAGE



SN54151A, SN54LS151, SN54S151 ... J OR W PACKAGE
SN74151A ... J OR N PACKAGE
SN74LS151, SN74S151 ... D, J OR N PACKAGE

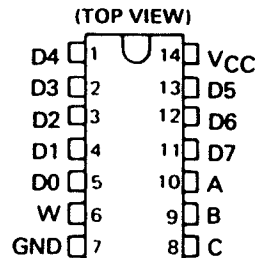


SN54LS151, SN54S151 ... FK PACKAGE
SN74LS151, SN74S151



NC - No internal connection

SN54152A, SN54LS152 ... W PACKAGE



For SN54LS152 Chip Carrier Information, Contact The Factory.

PRODUCTION DATA
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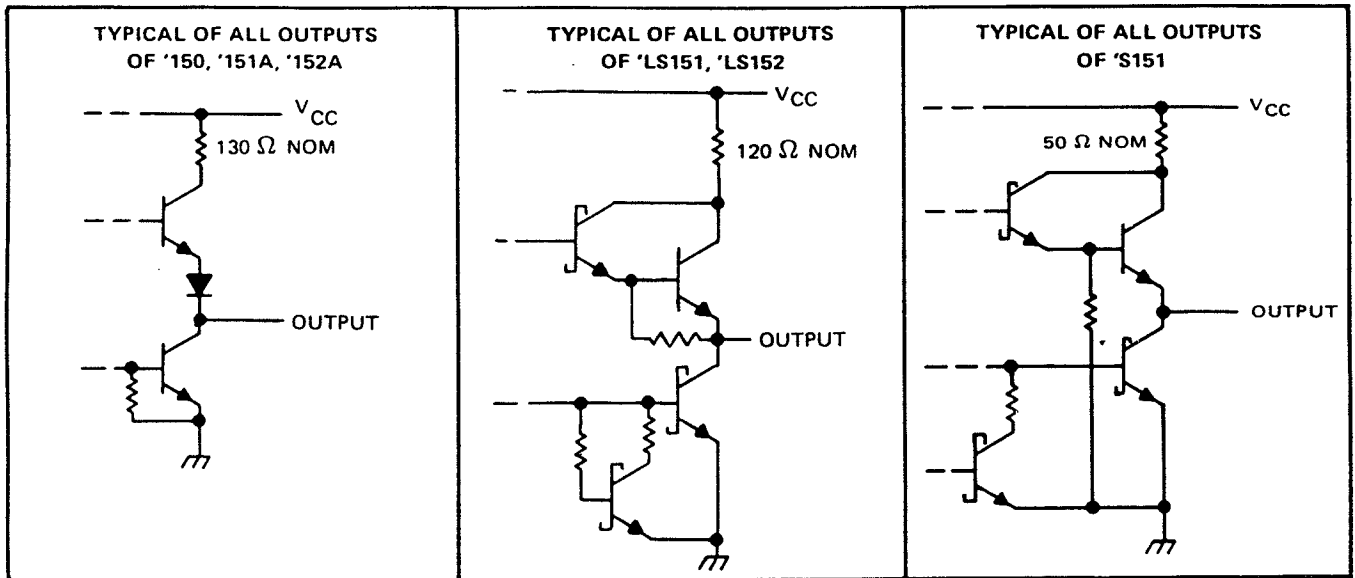
TEXAS
INSTRUMENTS

3

TTL DEVICES

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151
 SN74150, SN74151A, SN74LS151, SN74S151
 DATA SELECTORS/MULTIPLEXERS

schematics of inputs and outputs



logic

'150
 FUNCTION TABLE

INPUTS				STROBE \bar{G}	OUTPUT W
D	C	B	A		
X	X	X	X	H	H
L	L	L	L	L	$\bar{E0}$
L	L	L	H	L	$\bar{E1}$
L	L	H	L	L	$\bar{E2}$
L	L	H	H	L	$\bar{E3}$
L	H	L	L	L	$\bar{E4}$
L	H	L	H	L	$\bar{E5}$
L	H	H	L	L	$\bar{E6}$
L	H	H	H	L	$\bar{E7}$
H	L	L	L	L	$\bar{E8}$
H	L	L	H	L	$\bar{E9}$
H	L	H	L	L	$\bar{E10}$
H	L	H	H	L	$\bar{E11}$
H	H	L	L	L	$\bar{E12}$
H	H	L	H	L	$\bar{E13}$
H	H	H	L	L	$\bar{E14}$
H	H	H	H	L	$\bar{E15}$

'151A, 'LS151, 'S151
 FUNCTION TABLE

INPUTS			STROBE \bar{G}	OUTPUTS	
C	B	A		Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\bar{D0}$
L	L	H	L	D1	$\bar{D1}$
L	H	L	L	D2	$\bar{D2}$
L	H	H	L	D3	$\bar{D3}$
H	L	L	L	D4	$\bar{D4}$
H	L	H	L	D5	$\bar{D5}$
H	H	L	L	D6	$\bar{D6}$
H	H	H	L	D7	$\bar{D7}$

'152A, 'LS152
 FUNCTION TABLE

SELECT INPUTS			OUTPUT W
C	B	A	
L	L	L	$\bar{D0}$
L	L	H	$\bar{D1}$
L	H	L	$\bar{D2}$
L	H	H	$\bar{D3}$
H	L	L	$\bar{D4}$
H	L	H	$\bar{D5}$
H	H	L	$\bar{D6}$
H	H	H	$\bar{D7}$

H = high level, L = low level, X = irrelevant
 $\bar{E0}, \bar{E1}, \dots, \bar{E15}$ = the complement of the level of the respective E input
 $\bar{D0}, \bar{D1}, \dots, \bar{D7}$ = the level of the D respective input

TTI DEVICES

TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,
SN54S162, SN54S163, SN74160 THRU SN74163,
SN74LS160A THRU SN74LS163A, SN74S162, SN74S163
SYNCHRONOUS 4-BIT COUNTERS

OCTOBER 1976—REVISED DECEMBER 1983

'160,'161,'LS160A,'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162,'163,'LS162A,'LS163A,'S162,'S163 . . . FULLY SYNCHRONOUS COUNTERS

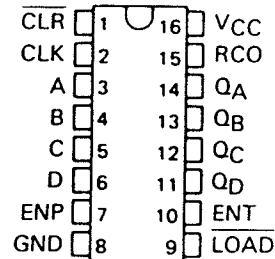
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE

SERIES 74' . . . J OR N PACKAGE

SERIES 74LS', 74S' . . . D, J OR N PACKAGE

(TOP VIEW)

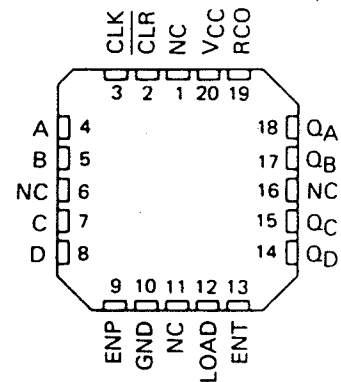


NC—No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE

SERIES 74LS', 74S'

(TOP VIEW)



NC—No internal connection

TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160,'162,'LS160A,'LS162A, and 'S162 are decade counters and the '161,'163,'LS161A,'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162,'163,'LS162A,'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

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TEXAS
INSTRUMENTS

TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

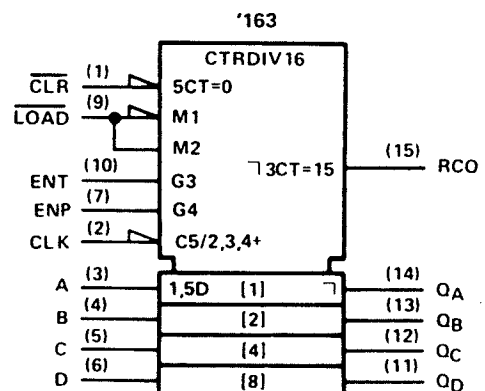
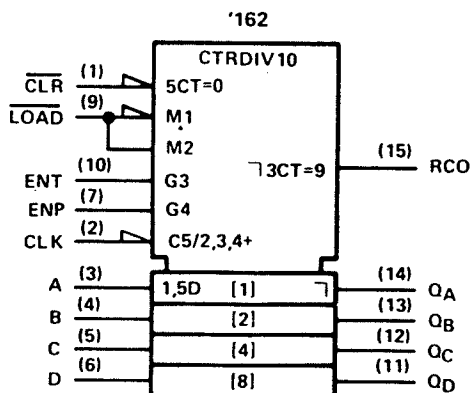
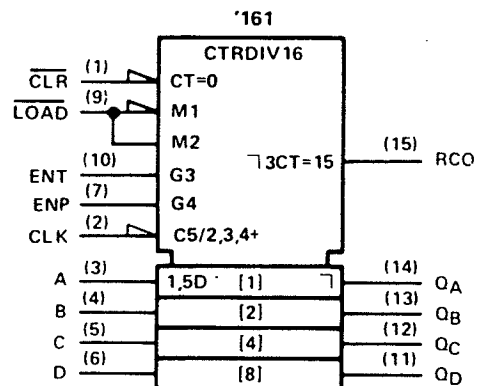
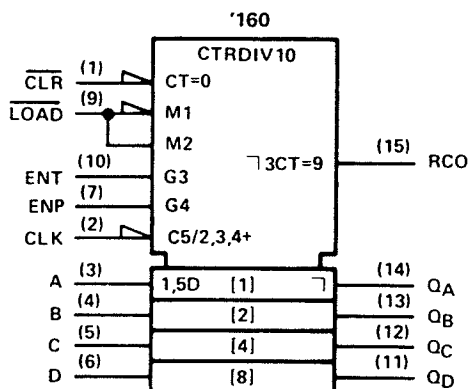
'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS160A thru 'LS163A are completely new designs. Compared to the original 'LS160 thru 'LS163, they feature 0-nanosecond minimum hold time and reduced input currents I_{IH} and I_{IL} .

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A or 'S163 will count in binary. Virtually any count mode (modulo-N, N_1 -to- N_2 , N_1 -to-maximum) can be used with this fast look-ahead circuit.

logic symbols



Pin numbers shown on logic notation are for D, J or N packages.

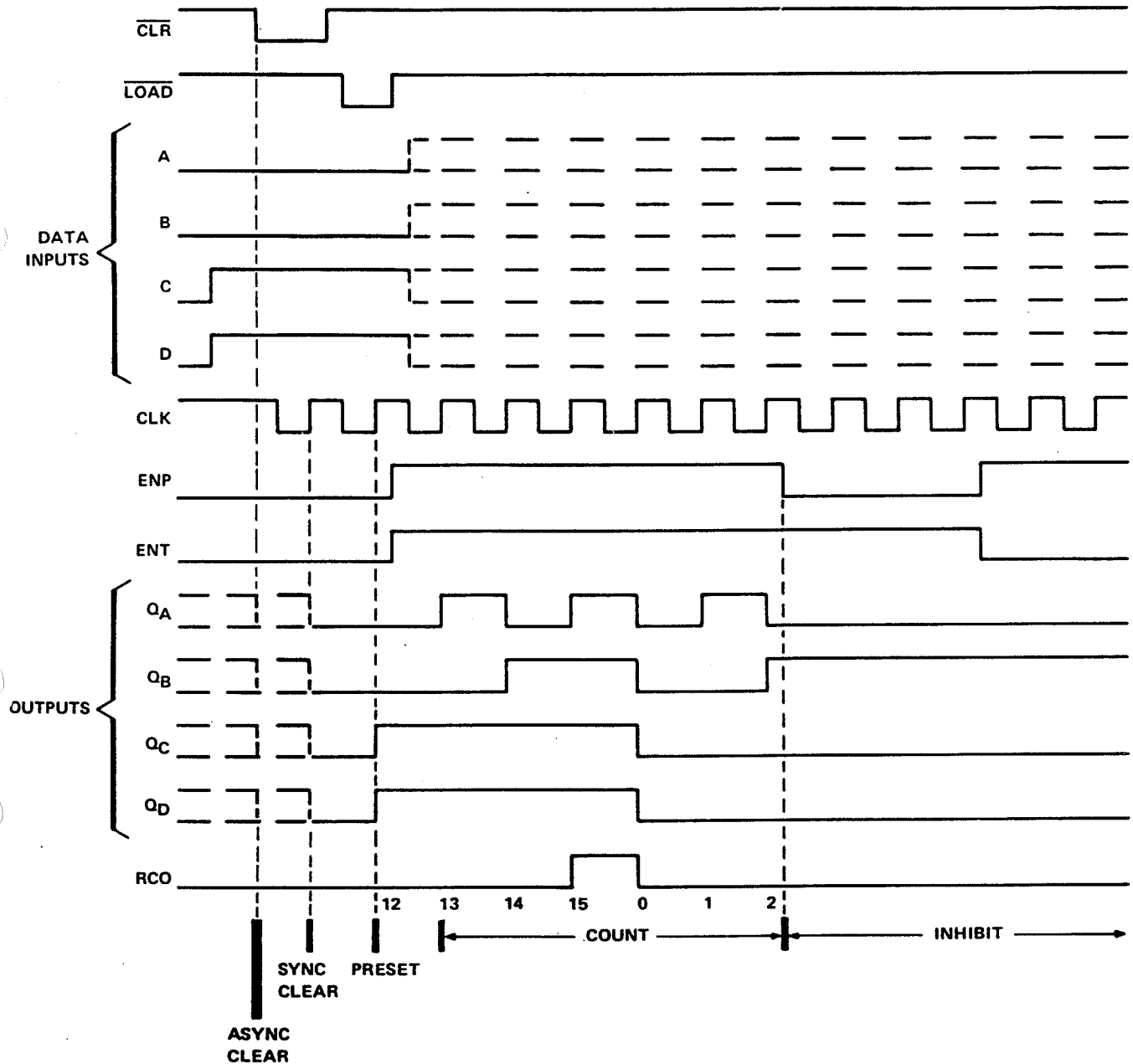
TYPES SN54161, SN54163, SN54LS161A, SN54LS163A, SN54S163,
 SN74161, SN74163, SN74LS161A, SN74LS163A, SN74S163
 SYNCHRONOUS 4-BIT COUNTERS

'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit

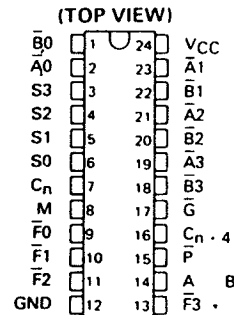


TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

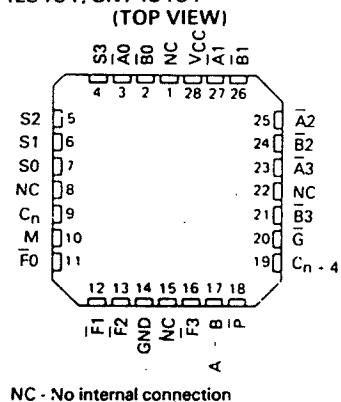
DECEMBER 1972 - REVISED DECEMBER 1983

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
 - Addition
 - Subtraction
 - Shift Operand A One Position
 - Magnitude Comparison
 - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
 - Exclusive-OR
 - Comparator
 - AND, NAND, OR, NOR
 - Plus Ten Other Logic Operations

SN54181, SN54LS181, SN54S181 ... J OR W PACKAGE
SN74181 ... J OR N PACKAGE
SN74LS181, SN74S181 ... DW, J OR N PACKAGE



SN54LS181, SN54S181 ... FK PACKAGE
SN74LS181, SN74S181



TYPICAL ADDITION TIMES

NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALU's
	USING '181 AND '182	USING 'LS181 AND '182	USING 'S181 AND 'S182	ARITHMETIC/LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	24 ns	24 ns	11 ns	1		NONE
5 to 8	36 ns	40 ns	18 ns	2		RIPPLE
9 to 16	36 ns	44 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	60 ns	68 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The '181, 'LS181, and 'S181 are arithmetic logic units (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54182, SN54S182, SN74182, or SN74S182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading '182 or 'S182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the '182 and 'S182.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

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TYPES SN54181, SN54LS181, SN54S181,
SN74181, SN74LS181, SN74S181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

description (continued)

The '181, 'LS181, and 'S181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	\bar{A}_0	\bar{B}_0	\bar{A}_1	\bar{B}_1	\bar{A}_2	\bar{B}_2	\bar{A}_3	\bar{B}_3	\bar{F}_0	\bar{F}_1	\bar{F}_2	\bar{F}_3	C_n	C_{n+4}	\bar{P}	\bar{G}
Active-high data (Table 2)	A ₀	B ₀	A ₁	B ₁	A ₂	B ₂	A ₃	B ₃	F ₀	F ₁	F ₂	F ₃	\bar{C}_n	\bar{C}_{n+4}	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is $A-B-1$, which requires an end-around or forced carry to provide $A-B$.

The '181, 'LS181, or 'S181 can also be utilized as a comparator. The $A = B$ output is internally decoded from the function outputs (F_0, F_1, F_2, F_3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ($A = B$). The ALU must be in the subtract mode with $C_n = H$ when performing this comparison. The $A = B$ output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S_3, S_2, S_1, S_0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S_0, S_1, S_2, S_3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74, 74LS, and 74S devices are characterized for operation from 0°C to 70°C .

signal designations

The '181, 'LS181, and 'S181 together with the '182 and 'S182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators (O) and the bars over the terminal letter symbols (e.g., \bar{C}) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at \bar{C} means "do carry" while a high means "do not carry".

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

TYPES SN54181, SN54LS181, SN54S181,
 SN74181, SN74LS181, SN74S181
 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

signal designations (continued)

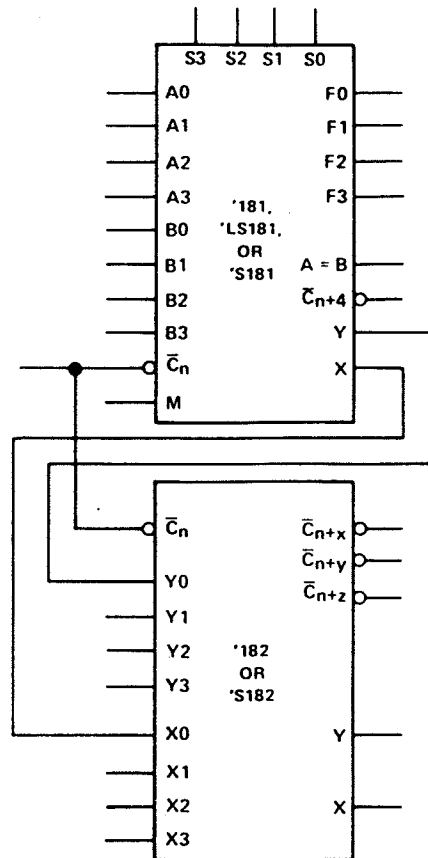


FIGURE 2

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0		$\bar{C}_n = H$ (no carry)	$\bar{C}_n = L$ (with carry)
L	L	L	L	$F = \bar{A}$	$F = A$	$F = A \text{ PLUS } 1$
L	L	L	H	$F = A + \bar{B}$	$F = A + B$	$F = (A + B) \text{ PLUS } 1$
L	L	H	L	$F = \bar{A}B$	$F = A + \bar{B}$	$F = (A + \bar{B}) \text{ PLUS } 1$
L	L	H	H	$F = 0$	$F = \text{MINUS } 1 \text{ (2's COMPL)}$	$F = \text{ZERO}$
L	H	L	L	$F = \bar{A}\bar{B}$	$F = A \text{ PLUS } \bar{A}\bar{B}$	$F = A \text{ PLUS } \bar{A}\bar{B} \text{ PLUS } 1$
L	H	L	H	$F = \bar{B}$	$F = (A + B) \text{ PLUS } \bar{A}\bar{B}$	$F = (A + B) \text{ PLUS } \bar{A}\bar{B} \text{ PLUS } 1$
L	H	H	L	$F = A \oplus B$	$F = A \text{ MINUS } B \text{ MINUS } 1$	$F = A \text{ MINUS } B$
L	H	H	H	$F = \bar{A}\bar{B}$	$F = \bar{A}\bar{B} \text{ MINUS } 1$	$F = \bar{A}\bar{B}$
H	L	L	L	$F = \bar{A} + B$	$F = A \text{ PLUS } AB$	$F = A \text{ PLUS } AB \text{ PLUS } 1$
H	L	L	H	$F = \bar{A} \oplus B$	$F = A \text{ PLUS } B$	$F = A \text{ PLUS } B \text{ PLUS } 1$
H	L	H	L	$F = B$	$F = (A + \bar{B}) \text{ PLUS } AB$	$F = (A + \bar{B}) \text{ PLUS } AB \text{ PLUS } 1$
H	L	H	H	$F = AB$	$F = AB \text{ MINUS } 1$	$F = AB$
H	H	L	L	$F = 1$	$F = A \text{ PLUS } A$	$F = A \text{ PLUS } A \text{ PLUS } 1$
H	H	L	H	$F = A + \bar{B}$	$F = (A + B) \text{ PLUS } A$	$F = (A + B) \text{ PLUS } A \text{ PLUS } 1$
H	H	H	L	$F = A + B$	$F = (A + \bar{B}) \text{ PLUS } A$	$F = (A + \bar{B}) \text{ PLUS } A \text{ PLUS } 1$
H	H	H	H	$F = A$	$F = A \text{ MINUS } 1$	$F = A$

3

TTL DEVICES