

Spartan-IIE Development Board User's Guide



1 Overview

The Spartan-IIE Development Kit provides a complete solution for developing designs and applications based on the Xilinx Spartan-IIE FPGA family. The kit bundles an expandable Spartan-IIE based system board with a power supply, user guide and reference designs. Also available from Insight, optional P160 expansion modules enable further application specific prototyping and testing. Xilinx ISE software and a JTAG cable are available as kit options.

The Spartan-IIE system board utilizes the 300,000 gate Xilinx Spartan-IIE device (XC2S300E-5FG456C) in the 456 fine-pitch ball grid array package. The high gate density and large number of user I/Os allows complete system solutions to be implemented in the low cost FPGA. The system board includes two clock sources, 82 user I/O header pins, an RS-232 port, LED displays, switches and additional user support circuits. An LVDS interface is provided, with 10-bit transmit and 10-bit receive ports, and clock signals for each. The board supports the Insight P160 expansion module standard, which allows application-specific expansion modules to be easily added.

The Spartan-IIE FPGA family has the advanced features needed to fit the most demanding, high volume applications. The Spartan-IIE Development Kit provides an excellent platform to explore these features so that you can quickly and effectively meet your time-to-market requirements.

2 The Spartan-IIE System Board

The Spartan-IIE System Board provides the FPGA, support circuits and the expansion slot for realizing advanced FPGA designs. Figure 1 shows a picture of the board and its features.

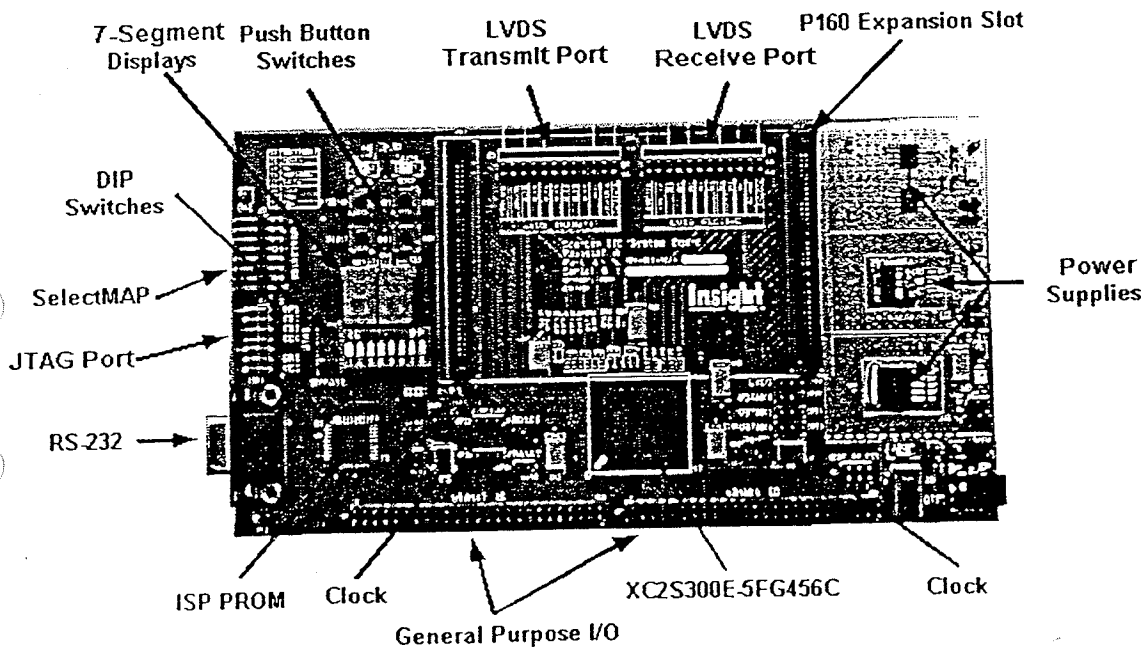


Figure 1 – Spartan-IIE System Board

3 Spartan-IIE Development Board Block Diagram

A high-level block diagram of the Spartan-IIE development board is shown in Figure 2 followed by a brief description of each sub-section.

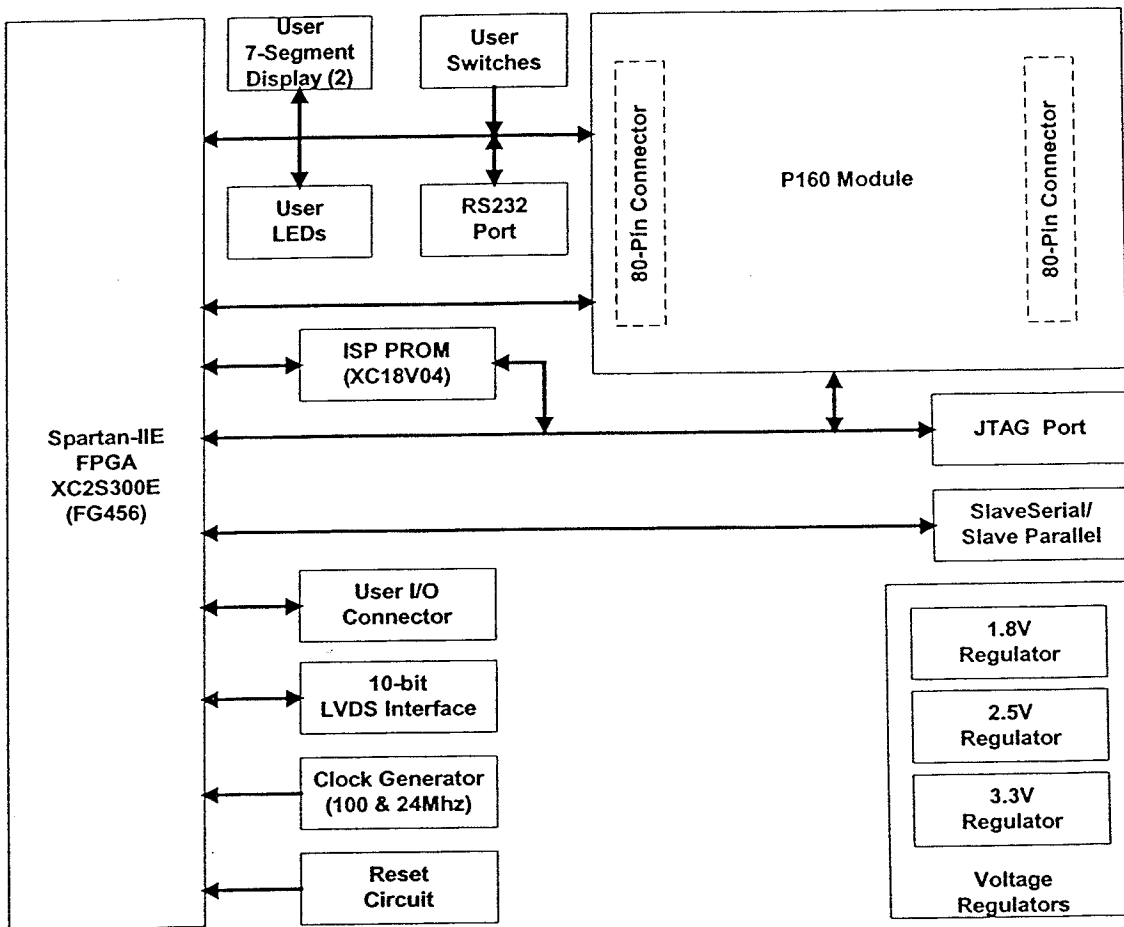


Figure 2 - Spartan-IIE Development Board Block Diagram

3.1 Spartan-IIE Device

The Spartan-IIE development board utilizes the Xilinx Spartan-IIE XC2S300E-FG456C. The Spartan™-IIE 1.8V Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The five-member family offers densities ranging from 50,000 to 300,000 system gates supporting 200Mhz designs and beyond.

Spartan-IIE devices deliver more gates, I/Os, and features per dollar than other FPGAs by combining advanced process technology with a streamlined architecture based on the proven Virtex™-E platform. Features include block RAM (up to 64K bits), distributed RAM (to 98,304 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

3.2 Clock Generation

The Spartan-IIE development board provides two master clock inputs to the Spartan-IIE FPGA. The following table provides a brief description of these clock signals.

Table 1 - Spartan-IIE development board Master Clocks

Signal Name	Spartan-IIE Pin #	Direction	Description
CLK.CAN2	AB12	Input	On-board 100 MHz Oscillator
CLK.CAN1	C11	Input	On-board 24 MHz Oscillator

The Spartan-IIE development board provides two on-board oscillators running at 100Mhz (CLK.CAN2) and 24Mhz (CLK.CAN1). The 100Mhz oscillator is enabled when the JP24 jumper is open, while leaving the JP32 jumper open will enable the 24Mhz oscillator.

3.3 Reset Circuit

The Spartan-IIE development board uses the TI TPS3125 voltage supervisory device to monitor the Spartan-IIE FPGA core voltage (1.8V). This circuit asserts a reset signal (RESET_n_FPGA) to the Spartan-IIE device when the 1.8V core voltage falls below its minimum specifications (1.71V). The reset signal to the FPGA is a fixed 100ms active low pulse. In addition to monitoring the core voltage, this circuit can be used to generate a reset pulse by activating the Master Reset (MR_n) signal to the TPS3125 device via the on-board push-button switch (SW3). The following figure shows the reset circuit on the Spartan-IIE development board.

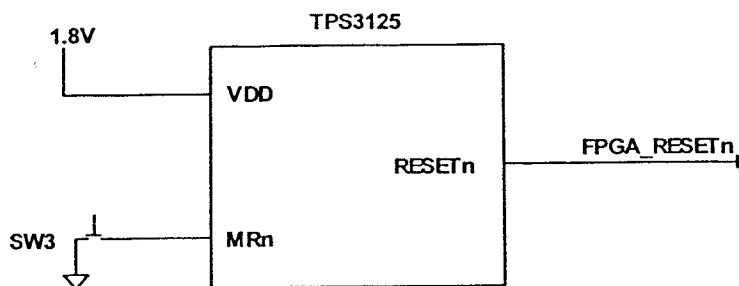


Figure 3 – Reset Circuit

3.4 User 7-Segment Display

The Spartan-IIE development board utilizes two common-cathode 7-segment LED displays that can be used during the test and debugging phase of a design. The user can turn a given segment on by driving the associated signal high. The following figure shows the user 7-segment display interface to the Spartan-IIE FPGA.

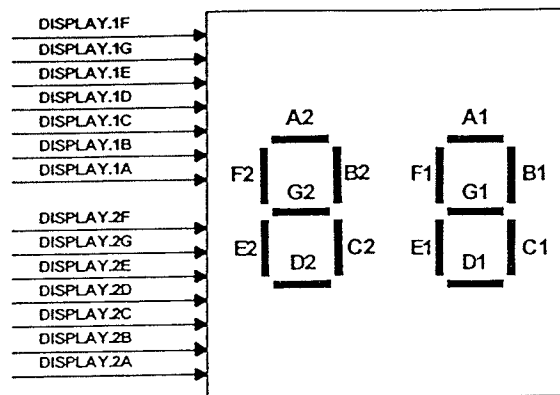


Figure 4 - 7-Segment LED Display Interface

3.4.1 7-Segment Display Signal Description

The following table shows the 7-Segment LED display pin descriptions.

Table 2 - 7-Segment Display Signal Descriptions

Signal Name	Spartan-II E Pin #	Description
DISPLAY.1A	D9	7-Segment LED Display1, Segment A
DISPLAY.1B	C9	7-Segment LED Display1, Segment B
DISPLAY.1C	F11	7-Segment LED Display1, Segment C
DISPLAY.1D	F9	7-Segment LED Display1, Segment D
DISPLAY.1E	F10	7-Segment LED Display1, Segment E
DISPLAY.1F	D10	7-Segment LED Display1, Segment F
DISPLAY.1G	C10	7-Segment LED Display1, Segment G
DISPLAY.2A	B9	7-Segment LED Display2, Segment A
DISPLAY.2B	A8	7-Segment LED Display2, Segment B
DISPLAY.2C	B8	7-Segment LED Display2, Segment C
DISPLAY.2D	E7	7-Segment LED Display2, Segment D
DISPLAY.2E	E8	7-Segment LED Display2, Segment E
DISPLAY.2F	E10	7-Segment LED Display2, Segment F
DISPLAY.2G	E9	7-Segment LED Display2, Segment G

3.5 User LED

The Spartan-II E development board provides a single user LED. Pin A9 of the Spartan-II E FPGA is used to drive this active low signal.

3.6 User Push Button Switches (SW5, and SW6)

The Spartan-II E development board design provides two user push button switch inputs to the Spartan-II E FPGA. Each push button switch can be used to generate an active low signal.

3.6.1 User Push Button Switch Signal Assignments

The following table shows the pin assignments for the user push button switches.

Table 3 - User Push Button Switch Signal Assignments

Signal Name	Spartan-IIE Pin #	Description
PUSH.USER1	D8	User Push Button Switch Input 1 (SW5)
PUSH.USER2	A6	User Push Button Switch Input 2 (SW6)

3.7 User DIP Switch (SW4)

The Spartan-IIE development board provides 8 user switch inputs. These switches can be statically set to a low or high logic level.

3.7.1 User DIP Switch Interface

The following figure shows the user DIP switch interface to the Spartan-IIE FPGA.

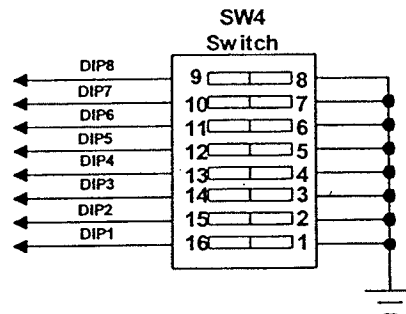


Figure 5 – User DIP Switch Interface

3.7.2 User DIP Switch Signal Assignments

The following table shows the user switch pin assignments.

Table 4 - User DIP Switch Signal Assignments

Signal Name	Spartan-IIE Pin #	Description
DIP8	D7	User Switch Input 8
DIP7	C6	User Switch Input 7
DIP6	D6	User Switch Input 6
DIP5	C5	User Switch Input 5
DIP4	A5	User Switch Input 4
DIP3	B5	User Switch Input 3
DIP2	A4	User Switch Input 2
DIP1	B4	User Switch Input 1

3.8 RS232 Port

The Spartan-IIE development board provides an RS232 port that can be driven by the Spartan-IIE FPGA. A subset of the RS232 signals is used on the Spartan-IIE development board to implement this interface (RD and TD signals).