EPC - EMBEDDED PARALLEL COMPUTING

B. Svensson[1], V. Gaspes[1], T. Larsson[1], H. Hoai-Bengtsson[2], J. Bengtsson[1],
A. Persson[1], Zain-ul-Abdin[1], P. Gelin[2], A. Wass[3], P. Ericsson[4], K. Lind[4], A. Åhlander[4]

1. Centre for Research on Embedded Systems, Halmstad University;
2. Combitech AB; 3. Ericsson AB; 4. Saab Microwave Systems

The project addresses the efficient use of parallel and reconfigurable computing structures in embedded high-performance applications. The industrial challenges for the research are, e.g., baseband processing in base stations for future mobile communication systems based on the LTE (long-term evolution) standard, and real-time image forming in synthetic aperture radar systems.

Keywords: Stream processing, Coarse-grain reconfigureable computing, Processor arrays, Parallel computation models, High-performance signal processing, Radio base-stations, Radar signal processing.

Purpose
Understanding parallel architectures and their usage is an important part of the CERES research program on Cooperating Embedded Systems. The project addresses the efficient use of parallel and reconfigurable computing structures in embedded high-performance applications.

Goals
The overall goals of the project are: (1) to understand which overall (hardware and software) architectures are best suited for a given application domain, and (2) to find efficient ways of writing programs / mapping applications that execute efficiently on parallel/reconfigurable computing systems. The project does not address general purpose processing; rather it is oriented towards the needs of high-performance embedded signal processing applications.
The Project has four main “threads", each with its own goal:

Thread 1
Stream processing architectures and languages with applications in baseband processing. Goal: To develop language based tools that enable efficient execution of baseband processing algorithms on programmable array architectures. (See Figure 1).

Thread 2
Programming of reconfigurable chip architectures. Goal: To explore well established computation models and devise new design methods based on these models to — for selected streaming application(s) — program the emerging class of reconfigurable chip architectures with varying granularity. (See Figure 2).

Thread 3
Methods for coordination of signal processing components. Goal: To develop methods for design of high performance signal processing software that is portable to several parallel platforms.

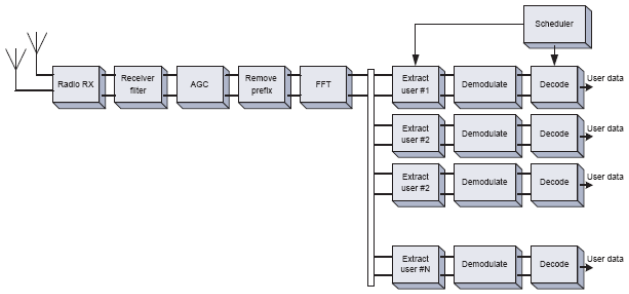

Figure 1: A simplified modular view of the principal functions of the baseband receiver in long term evolution (LTE) radio base stations

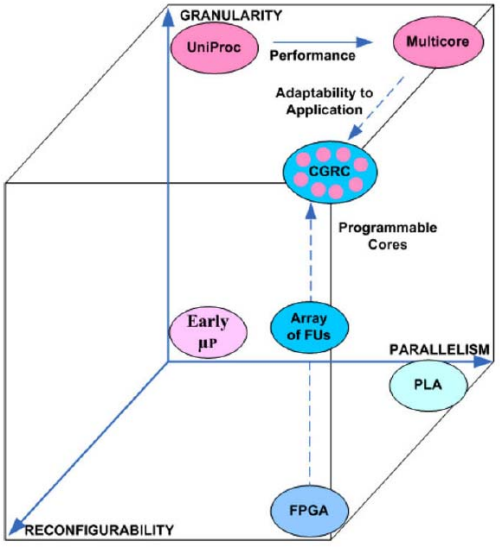

Figure 2: The development of the coarse-grained reconfigurable computing (CGRC) paradigm.

Thread 4
Studies of realization of challenging signal processing applications. Typical for the applications in question is that it is initially unknown whether it is at all possible to meet their demands with state-of-the-art technology or foreseeable new technology. Goal: For particular such application(s), acquire understanding of the demands on computer architectures, and possibly propose architecture solutions.

RESULTS

Among the results so far are:
Models for manycore performance evaluation. A machine model that captures essential performance measures of array structured, tightly coupled manycore processors has been developed. A timed intermediate representation has been constructed, and, by means of abstract interpretation, this can be executed in order to obtain feedback about the run-time behaviour of the application (see Figure 3).

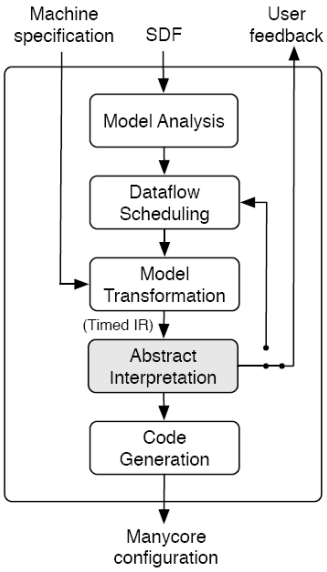

Figure 3: Framework for code mapping using abstract interpretation of timed configuration graphs.

CSP based programming of reconfigurable processor arrays. An approach of compiling a CSP based language, `occam-pi`, to a reconfigurable processor array has been evaluated. The method is based on developing a compiler backend for generating native code for the target architecture. The new parallel architecture from Ambric has been used as target.

PARTNERS AND STATUS

Industrial Partners: Combitech AB, Ericsson AB (2007-2008), Saab Microwave Systems.

Associated partners: Ambric, Inc., Portland, OR, USA; UC Berkeley, CA, USA.

Project funding: CERES profile funding from the Knowledge Foundation, together with the industrial partners' efforts in the project.

Project duration: June 2007 – May 2010.
Project leader is Bertil Svensson, CERES.

PUBLICATIONS

Bengtsson, J. and B. Svensson, "Manycore performance analysis using timed configuration graphs", *2009 IEEE International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS IX)*, Samos, Greece, July 20-23, 2009.

Larsson, T., "A two level approach to the design of software for cooperating embedded systems", *Proc. of 7th IEEE International Conference on Industrial Informatics (INDIN 2009)*, Cardiff, UK, 24-26 June, 2009.

Bengtsson, J., *Models and Methods for Development of DSP Applications on Manycore Processors*, PhD Thesis, Halmstad University and Chalmers University of Technology, June 2009.

Zain-ul-Abdin and B. Svensson, "Evolution in architectures and programming methodologies of coarse-grained reconfigurable computing", *Microprocessors and Microsystems* 33 (2009) 161—178.

Bengtsson, J. and B. Svensson, "A domain-specific approach for software development on multicore platforms", *Computer Architecture News*, December 2008.

Zain-ul-Abdin, *High-Level Programming of Coarse-Grained Reconfigurable Architectures*, Licentiate Thesis, Halmstad University and Örebro University, December 2008.

Zain-ul-Abdin and B. Svensson, "Using a CSP based programming model for reconfigurable processor arrays," *Proc. of 2008 International Conference on ReConFigurable Computing and FPGAs (ReConFig'08)*, Cancun ,Mexico, Dec. 3-5, 2008.

Bengtsson, J. and B. Svensson, "Methodologies and Tools for Development of Signal Processing Software on Multicore Platforms", *Workshop on Streaming Systems in conjunction with the 41st Annual IEEE/ACM International Symposium on Michroarchitecture (MICRO)*, Como ,Italy, November 8-9, 2008.

Jerker Bengtsson, Verónica Gaspes and Bertil Svensson, "Machine Assisted Code Generation for Manycore Processors," *Proc. of the 9th biennial SNART Conference on Real-Time Systems (Real-Time in Sweden – RTiS'07)*, Västerås, Sweden, Aug. 21-22, 2007, pp. 164-172.

Chaudhry Majid Ali and Muhammad Qasim, "Signal Processing on Ambric Processor Array: Baseband processing in radio base stations", Master's Thesis in Computer Systems Engineering, Technical report, IDE0838, June 2008

J. Bengtsson, A Model Set for Manycore Performance Evaluation Through Abstract Interpretation of Timed Configuration Graphs," Tech. Rep. IDE0856, School of Information Science, Computer and Electrical Engineering, 2008.

Åhlander, A., B. Svensson, H. Hellsten, K. Lind, and J. Lindgren "Architectural challenges in memory-intensive, real-time image forming" *Proc. 36th Annual International Conference on Parallel Processing*, XiAn, China, Sept. 10-14, 2007.