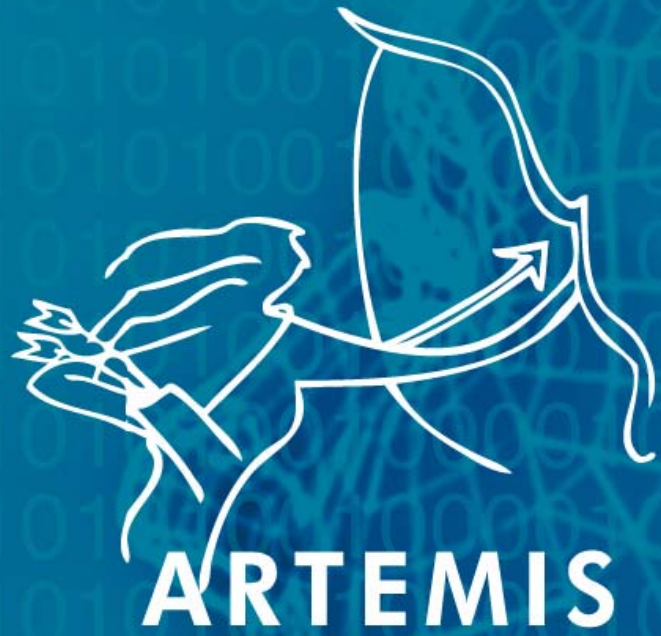
ARTEMISIA ASSOCIATION

The association for R&D actors in the field of ARTEMIS



SMECY

Smart Multicore Embedded Systems

Advanced Research & Technology for EMbedded Intelligence and Systems

Introduction

- **Mission**
  - Develop new programming technologies enabling the exploitation of many (100s) core architectures
- **Key Outcomes**
  - Programming and design methods
  - Multi-core programmable architectural solutions
  - Associated supporting tools
  - Evaluation in selected applications
- **Competence Goal**
  - Understand holistic integration of
    - multi-core SoC design
    - embedded software
  - Master smart system design for future applications
    - consumer, wireless, communication and transportation

Application Focus

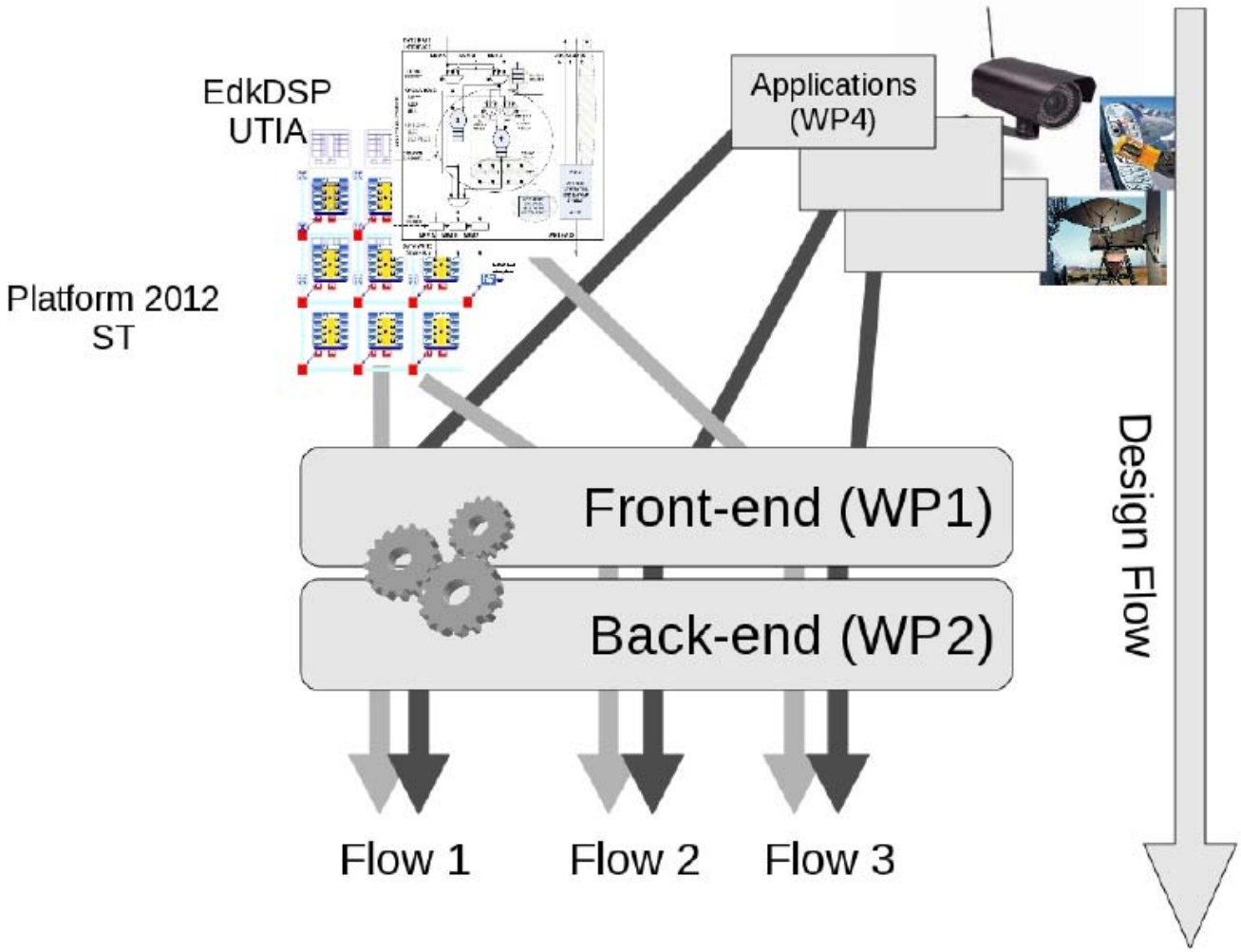
- Massive real-time data-processing found in the domains of
  - consumer electronics
    - e.g., video surveillance and HD video codecs
  - telecommunications
  - transportation
    - e.g., automotive, avionics and radar

- The results of SMECY will be driven by and demonstrated in a number of industry cases from these domains
- This will cover industrial applications as well as industrial platforms

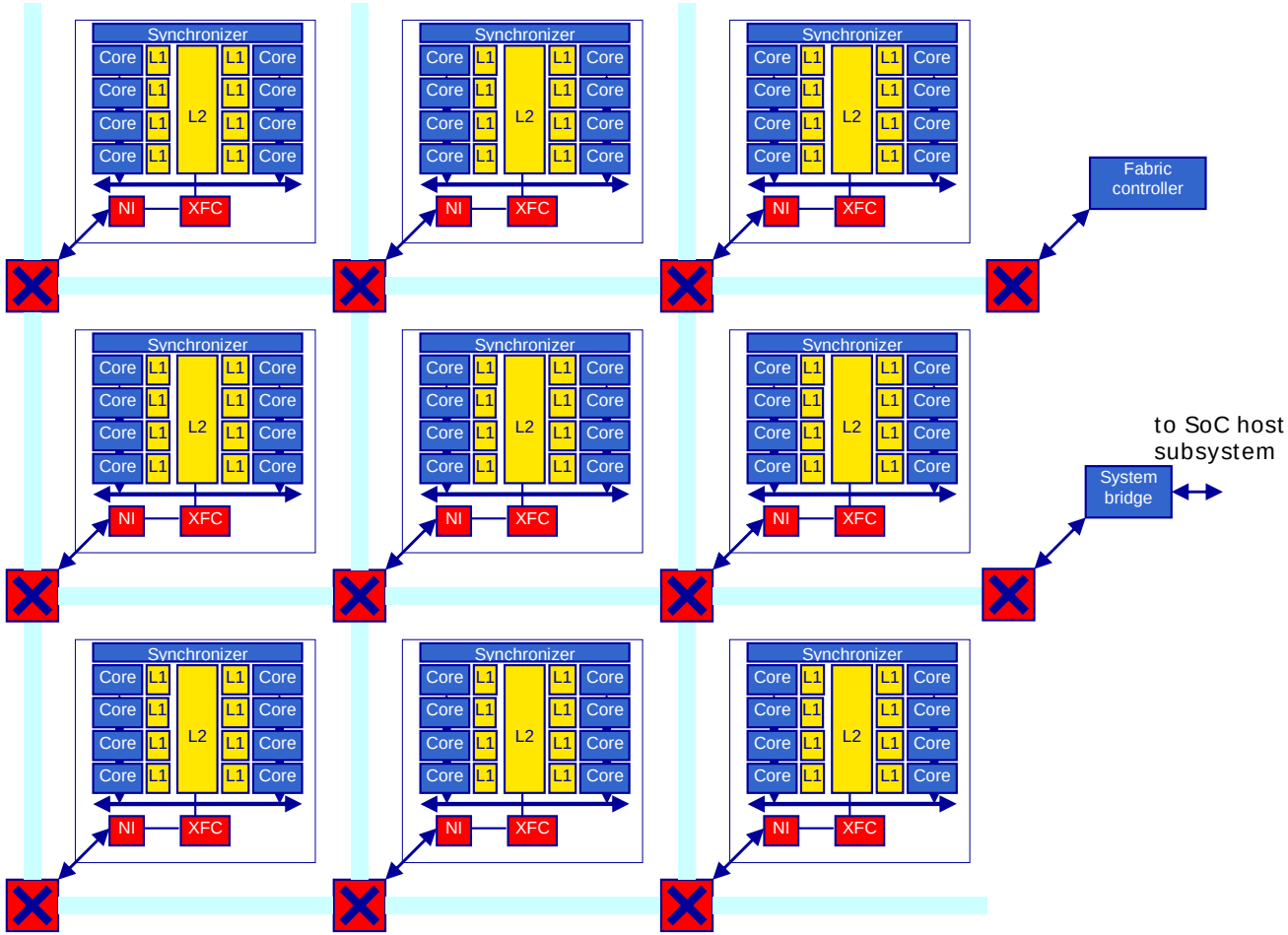
SMECY Partners

Country	*Industrial partners (19)*	*Short name*	*Academic partners (11)*	*Short name*
France	CEA	CEA	Université Joseph Fourier Grenoble 1	UJF/Verimag
	Thomson Gras Valley France	GVF		
	HPC Project	HPC		
	SKYLAB Industries	SKYLAB		
	STMicroelectronics (Grenoble 2)SAS	ST-GNB2		
	Thales Research & Technology (FR)	TRT-FR		
Netherlands	ACE Associated Compiler Experts bv	ACE	Technische Universiteit Delft	TUDelft
	Philips Medical Systems	PMS		
Greece	Hellenic Aerospace Industry S.A.	HAI	Aristotle University of Thessaloniki	AUTH
			University of Ioannina	UOI
Czech Rep.	CIP plus s.r.o.	CIP	Brno University of Technology	BUT
			Czech Academy of Sciences	UTIA
Denmark			Danmarks Tekniske Universitet	DTU
Sweden	Free2move AB	F2M	Högskolan i Halmstad	HH
	Realtime Embedded AB	RTE		
	Saab Microwave Systems	SMW		
Italy	SELEX SISTEMI INTEGRATI	SELEX-SI	Politecnico di Milano	POLIMI
	STMicroelectronics S.r.l.	ST Italy	Politecnico di Torino	POLITO
			Universita di Bologna	UNIBO
Finland	Nethawk Oyj	NetHawk		
	Tellabs Oy	Tellabs		
	VTT	VTT		
United Kingdom	Thales Research & Technology (UK)	TRT-UK		

SMECY Conceptual Approach



Platforms: P2012 (STMicroelectronics)



Platforms: UTIA EdkDSP platform

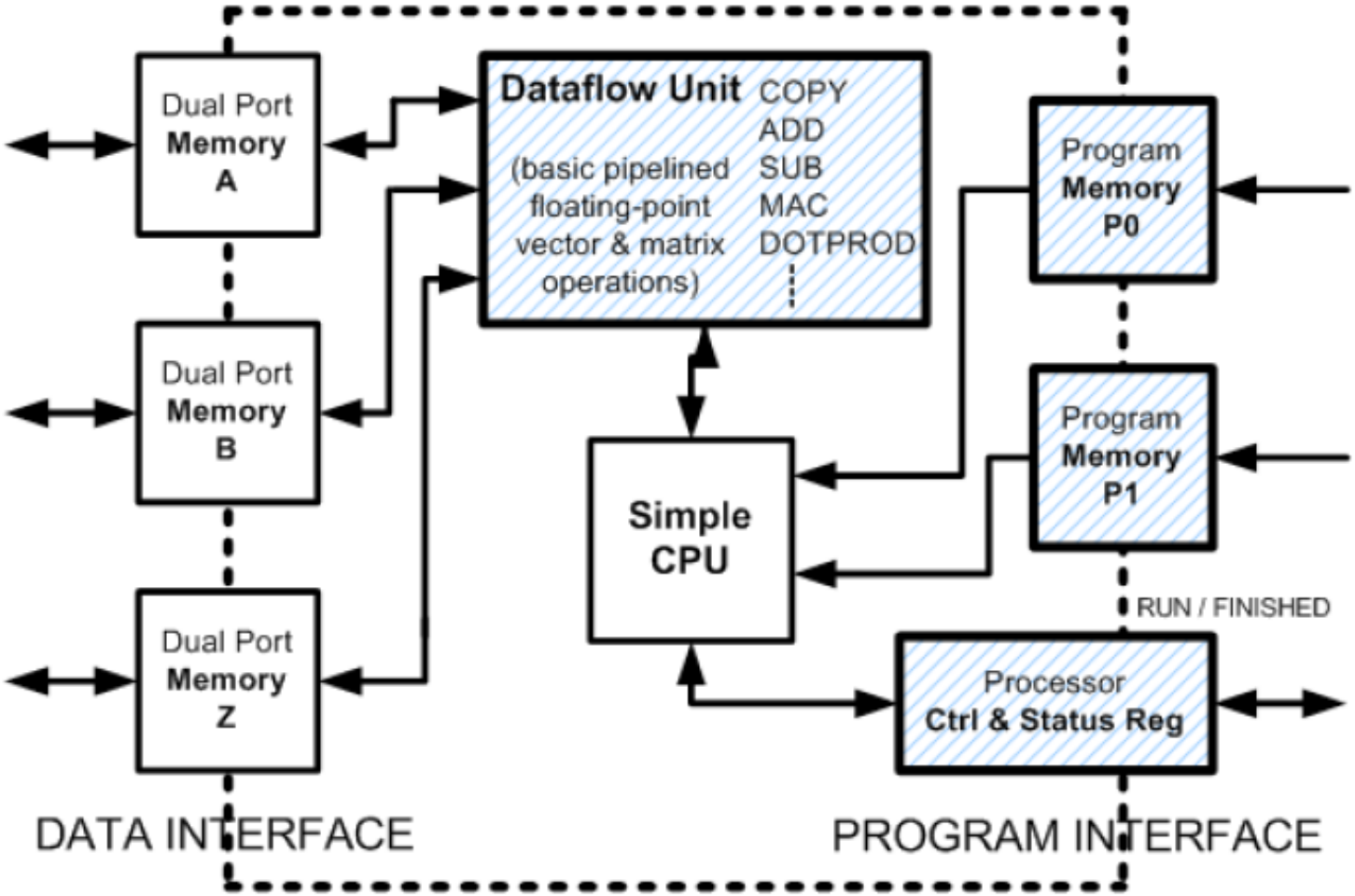


Figure 10: Basic computing element.

Platforms: UTIA EdkDSP platform (cont'd)

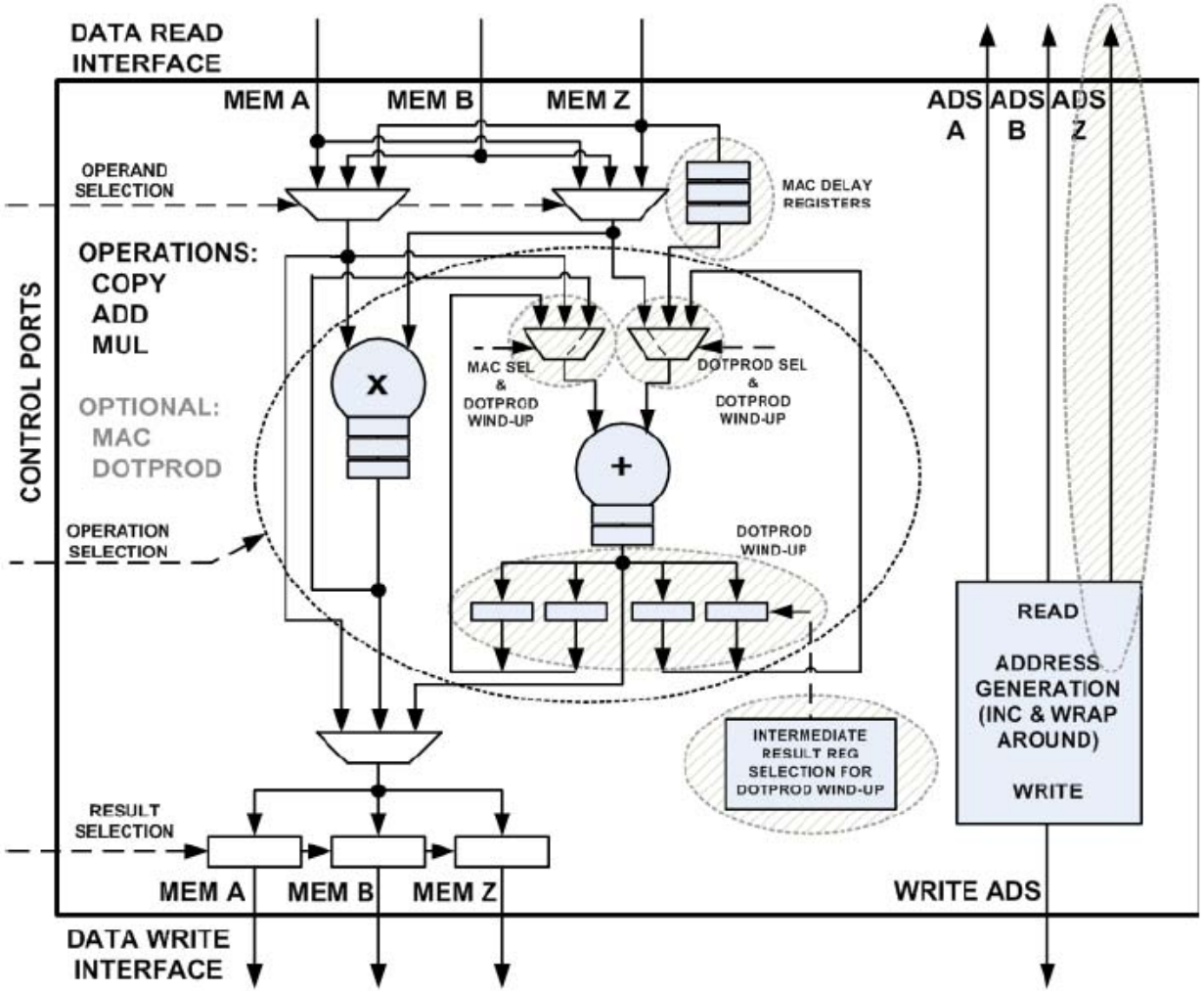


Figure 11: Structure of the EdkDSP

WP1 Application mapping and exploration

- Programming models,
- Optimisation and design space exploration methods and tools
- Requirements and characteristics of
  - a set of application types (from WP4)
  - a set of multi-core platform types (from WP3).

- Tasks
  - T1.1 Application and programming model
  - T1.2 Design space exploration.
  - T1.3 Intermediate representation
  - T1.4 Data/control transformation and optimisation

- Swedish participation: F2M, HH

WP2 Multi-core code generation

- Methods and tools for platform dependent optimisation and execution code generation
  - taking into account
    - application constraints
    - multi-core platform

- Tasks
  - T2.1 Analysis for application constraints propagation and platform dependent parameters extraction
  - T2.2 Platform dependent optimization
    - Data sharing / Interconnection, Memory map, HW constraints management
  - T2.3: Execution code generation

- Swedish participation: None

WP3 HW/SW Architecture Innovative Concepts

- Innovative solutions for
  - Programmability
  - Virtualization
  - Acceleration of parallel execution
  - Runtime execution support

- Tasks
  - T3.1 Multi-core architecture for programmability and predictability (new features that make programming easier)
  - T3.2 Virtualization, composability and execution model
  - T3.3 Acceleration of parallel execution
  - T3.4 Runtime execution supporting fault tolerance, reliability and dynamic reconfiguration

- Swedish participation: HH, RTE

WP4 Application domains

- Case studies in various application domains with the purpose of:
  - defining requirements and constraints
  - performing validation, assessment and evaluation of method, tool and architecture solutions
    - at mid-term and towards the end of the project

- Tasks
  - T4.1 Radar signal processing and earth observation
  - T4.2 Multimedia, mobile and wireless transmission
  - T4.3 Stream processing (Video surveillance)
  - T4.4 Benchmarking and Cross-Validation

- Swedish participation: SMW, F2M, HH

Some figures

- Number of partners: 30
  - 19 industrial, 11 academic
- Number of countries: 9
- Number of person-months: 1915 (= 160 person-years)
- Total budget: 20 399 K€
  - EU funding: 3 406 K€
  - National funding: 6 474 K€
  - Partners' own funding: 10 519 K€
- Project duration: 36 months