ABSTRACT CERES seminar May 4, 2009

Some Glimpses of NoC Research at Jönköpings Tekniska Högskola (JTH)

Network on Chip paradigm is getting universal acceptance as the best option for meeting the interconnection and communication requirements of complex multi-core systems on chip. Jönköping university has been involved in focused research in various aspects of NoC based system design including NoC architectures and Mapping and Scheduling of Applications on NoC platforms. In this seminar, we will focus on our recent contributions in the area of Routing Algorithms for mesh topology NoCs. In particular, we will focus on the new concepts of Application Specific Routing algorithms and our recent work on Hierarchical NoCs and Deadlock free Hierarchical Routing. We will show how information regarding application's communication profile can be used to specialize an efficient routing algorithm for the application. We will also describe how larger NoCs can be built by reusing and connecting many sub-networks. This will give the designer to raise the level of reuse from a core to already designed NoCs. We also discuss solution to a new challenging problem in building hierarchical NoCs, namely design of deadlock free routing algorithm for a heterogeneous hierarchical network.

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