High-Level Programming of Coarse-Grained Reconfigurable Architectures

Abstract

The design of high-performance embedded systems for signal processing applications is facing the challenges of not only increased computational demands but also increased demands for adaptability to future functional requirements for these applications. A category of reconfigurable architectures consisting of program control-led processing units is gaining attention as a means to cope with these problems. This thesis focuses on the programming aspects for such coarse-grained reconfigurable computing devices and the relevant computation models capable of exposing different kinds of parallelism inherent in the application. Thus these computation models can be adopted for expressing computations intended for such machines in order to achieve better performance.

The field of coarse-grained reconfigurable architectures is first explored, and based on the architectural variations in terms of granularity, reconfigurability, and interconnection networks, coarse-grained reconfigurable architectures are classified into four categories. The categories are hybrid architectures, arrays of functional units, arrays of processors, and arrays of soft processors. A study of the programming methodologies used for these different architectures reveals that programming techniques based on computation models such as Stream processing, Communicating Sequential Processes (CSP), and Kahn Process Networks (KPN) are gaining wider acceptance.

Our hypothesis is that the use of languages based on appropriate model of computation enhances the productivity and allows better use of resources without compromising performance. As a proof of concept, experimental studies are performed based on CSP as a selected model of computation. The rst study involves a concurrent language, which is used to generate descriptions for FPGAs. In the second, an approach of compiling a CSP based language, occam-pi, to a reconfigurable processor array is evaluated. The method is based on developing a compiler backend for generating native code for the target architecture.

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